Research Inventy: International Journal of Engineering And Science
Vol.6, Issue 1 (January 2016), PP -41-48
Issn (e): 2278-4721, Issn (p):2319-6483, www.researchinventy.com

Nine-Level Diode Clamped Asymmetric Dual Converter Based Statcom with Dc Link Voltage Control

M Rakesh*A Venkat Reddy**
, EEE Department, SreeDattha Institute of Engineering & Science*

Abstract: *Static synchronous compensators (STATCOMs) provide a power-electronics-based means of embedded control of transmission-line voltage and power flows. The integration of multilevel inverter to a STATCOM can extend traditional STATCOM capabilities to two way power flow control. This paper gives an overview of multilevel dual converter based STATCOMs with a focus on achieving minimum harmonic distortion and reasonable power quality improvement. The dual converter consists of two converters with different voltages to supply/absorb reactive power to/from the grid. The controller used in the STATCOMs can balance individual dc capacitor voltages when H-bridges run with different switching patterns and have parameter variations[1]. Reduced component count, simpler layout for switches, and smaller dc-link capacitor values are the attractive features of the proposed topology over the cascaded multilevel converters[2]. In extension to this the proposed system with STATCOM is designed with nine-level diode clamped multilevel inverter with sinusoidal PWM.*

Index Terms: *Diode-clamped inverter, cascaded inverters, voltage source converter(VSC), Pulse width modulation (PWM), cascaded Multi cell inverter, static compensator (STATCOM).*

I. Introduction

The ever-rising demand for electrical energy and depleting fossil fuel reserves are compelling reasons to use existing resources more efficiently. New highly efficient power electronic technologies and proper control strategies are therefore needed to reduce energy waste and to improve power quality. There is a great potential for improving the control strategy of the STATCOMS systems. Normally multipulse-converter-based and multilevel converter- based solutions are used for high-power applications. A multipulse converter uses more than one voltage source converter (VSC), with common dc link, operating with nearly fundamental switching frequency, and the output of each module is connected in series through the multipulse transformer. By adjusting the triggering pulses of different VSCs, specified total harmonic distortion (THD) of the injected current is achieved with reduced switching losses as compared to that of single-VSC-based solution. Cascaded multilevel inverters are based on a series connection of several single-phase inverters. This structure is capable of reaching medium output voltage levels using only standard low-voltage mature technology components. Typically, it is necessary to connect three to ten inverters in series to reach the required output voltage.

These converters also feature a high modularity degree because each inverter can be seen as a module with similar circuit topology, control structure, and modulation .THD without switching semiconductor devices at a high frequency. The two most commonly used schemes are diode clamped and cascaded converter topologies. The diode clamped multilevel topology is mostly restricted to a three-level configuration because of the complex layout of the diodes (which grows as the square of the number of levels) and the need for capacitor voltage balancing. To address some of the afore mentioned limitations in multilevel converters, a four-level open-ended-transformer-based multilevel converter, shown in Fig. 1 enables easier structural layout and reduced driver circuit complexity.

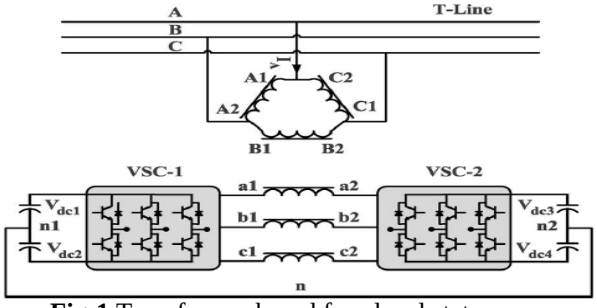

Fig-1 Transformer based four level statcom

To address this limitation, an asymmetric dual converter topology is proposed in this paper where in only two dc links are used without split-capacitor arrangement, as shown in Fig. 2. Furthermore, the THD of currents supplied to the grid is reduced by selecting a suitable ratio of dc-link voltages of the two VSCs. A ratio of 1:0.366 is selected based on the study of open-ended induction motor drive, which has similar power circuit configuration [2].

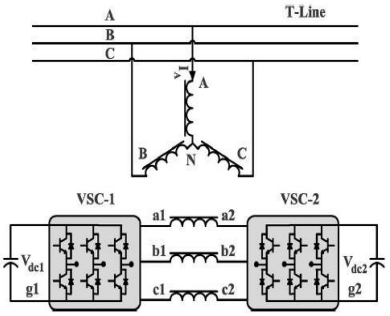

Fig-2 Asymmetric twin converter based statcom

II. Proposed Multilevel Converter

A.Principle of Operation

In the Asymmetric dual converter based statcom uses two converters having different voltage level. So the low voltage side voltage is the difference of two converter side voltages, similarly the HV side voltages is the sum of two converter voltages. Leakage inductances of the transformers act as input filter inductances of the STATCOM. Voltages appearing on the LV windings of the transformer are written in terms of output voltages of VSCs as

$$e_a = e_{a1g1} - e_{a2g2} + e_{g1g2}$$
$$e_b = e_{b1g1} - e_{b2g2} + e_{g1g2}$$
$$e_c = e_{c1g1} - e_{c2g2} + e_{g1g2} \qquad (1)$$

Where e_a, e_{a2g2}, and e_{g1g2} are the voltages across the LV winding of phase-a, the pole voltage of VSC-1, the pole voltage of VSC-2, and the voltage difference between negative dc-link terminals of the two VSCs, respectively. Since both VSCs have separate dc links, the sum of the LV winding phase currents should be zero.

$$i_a + i_b + i_c = 0 \qquad (2)$$

Furthermore, the sum of instantaneous values of grid voltages is equal to zero

$$v_A + v_B + v_C = 0 \qquad (3)$$

The sum of the LV winding voltages is given by

$$e_a + e_b + e_c = \frac{N_{LV}}{N_{HV}}(v_A + v_B + v_C) - r(i_a + i_b + i_c) - L\frac{d(i_a+i_b+i_c}{dt} \qquad (4)$$

where r and L are the resistance and leakage inductance as measured from the LV side, respectively, and NLV/NHV is the turns ratio. Substituting (2) and (3) into (4) gives.

$$e_a + e_b + e_c = 0 \qquad (5)$$

Substituting LV voltages from (1) in (5) results in

$$e_{g1g2} = -\frac{1}{3}(e_{a1g1} - e_{a2g2}) - \frac{1}{3}(e_{b1g1} - e_{b2g2}) - \frac{1}{3}(e_{c1g1} - e_{c2g2}) \qquad (6)$$

Substituting the value of $eg1g2$ in (1) yields

$$\begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} e_{a1g1} - e_{a2g2} \\ e_{b1g1} - e_{b2g2} \\ e_{c1g1} - e_{c2g2} \end{bmatrix} \qquad (7)$$

The relation between LV winding voltages and pole voltages is expressed in (7). The ratio of dc-link voltages of VSCs Vdc1 :Vdc2 should be equal to 1:0.366 for better performance. The line voltages of the LV side eab, ebc, and eca are expressed as pole voltages using (1)

$$e_{ab} = e_a - e_b = e_{a1g1} - e_{a2g2} - e_{b1g1} + e_{b2g2}$$
$$e_{bc} = e_b - e_c = e_{b1g1} - e_{b2g2} - e_{c1g1} + e_{c2g2}$$
$$e_{ca} = e_c - e_a = e_{c1g1} - e_{c2g2} - e_{a1g1} + e_{a2g2}$$

(8)

B. PWM Strategy

The switching state is decided by the modulating waveform and the PWM strategy used. Selective harmonic elimination method (SHEM), space vector modulation (SVM), or carrier-based PWM (CB-PWM) techniques are commonly used for high-power applications. SHEM is limited in use because of its slow dynamic response. Realization of SVM for multilevel converter requires an algorithm for the identification of sector. The presence of large number of sectors makes the implementation complex [5]. Hence, the use of phase-shifted (PS) CB-PWM is suggested for the proposed topology. This PWM technique expects the controller to generate individual modulating waveforms for each inverter output e_{a1g1}, e_{b1g1}, e_{c1g1}, e_{a2g2}, e_{b2g2}, and e_{c2g2}. Each modulating waveform is compared with a carrier waveform to determine the switching state of the corresponding inverter devices. This is similar to the PS CB-PWM technique used in H-bridge cascaded converters [6], [7]. For two H-bridges per phase, the resultant waveform of ac voltages is the sum of individual converter voltages. Therefore, carrier Waveforms are 180◦ PS from each other to cancel the carrier frequency harmonics.

III. Development Of The Equivalent

CIRCUIT OF THE SYSTEM

For the purpose of analysis, an equivalent circuit of the proposed STATCOM is derived and is shown in Fig. 7. Transformer is represented by equivalent series combination of inductances, resistances, and voltage sources. To model the losses in two VSCs, two resistances r1 and r2 are placed in parallel to the two dc links. The governing equations of the proposed system can be derived a equations

$$S\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} = \begin{pmatrix} \frac{-r\omega_b}{L} & 0 & 0 \\ 0 & \frac{-r\omega_b}{L} & 0 \\ 0 & 0 & \frac{-r\omega_b}{L} \end{pmatrix} \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} + \frac{\omega_b}{L} \begin{pmatrix} -e_a + V_a \\ -e_b + V_b \\ -e_c + V_c \end{pmatrix} \qquad (9)$$

The following equation gives the power balance condition between the ac and dc links of VSC-1:

$$v_{dc1} i_{dc1} = \frac{3}{2}\left(e_{d1} i_d + e_{q1} i_q \right) \qquad (10)$$

The current flowing through the dc-link capacitor c1 is related to the dc-link voltage vdc1 as follows

$$s v_{dc1} = \omega_b c_1 \left(i_{dc1} - \frac{v_{dc1}}{r_1} \right) \qquad (11)$$

where $C1$ is defined as $1/(\omega bc1zbase)$. Substituting $idc1$ from (11)

$$s v_{dc1} = \omega_b c_1 \left(\frac{3}{2v_{dc1}} \left(e_{d1} i_d + e_{q1} i_q \right) - \frac{v_{dc1}}{r_1} \right) \qquad (12)$$

Similarly, the governing equation for VSC-2 is expressed as

$$s v_{dc2} = \omega_b c_2 \left(\frac{-3}{2v_{dc2}} \left(e_{d2} i_d + e_{q2} i_q \right) - \frac{v_{dc2}}{r_2} \right) \qquad (13)$$

Equations (10), (13), and (14) represent the behavior of the system. These equations are used in the following section.

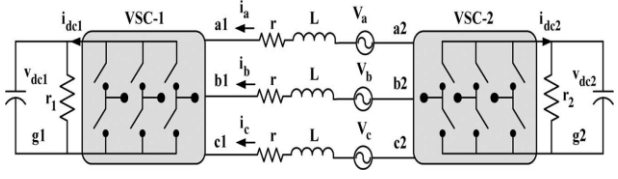

Fig-3 Equivalent circuit diagram of the proposed STATCOM

IV. Development Of The Controller

In this Asymmetric dual converter based STATCOM we are using two dc link voltage V_{dc1} & V_{dc2}.The controller must regulate the dc link voltages and calculate the total reactive power flowing to/from the STATCOM.

A. Current Control

Control variables x_1 and x_2 govern the system currents i_d and i_q, respectively, as per the differential equation. Therefore, current control is achieved by controlling variables x_1 and x_2 using the errors between reference values and actual currents, as given by

$$x_1 = k_{p1}(i_{d\_ref} - i_d) + k_{i1}\int(i_{d\_ref} - i_d)dt \qquad (14)$$

$$x_2 = k_{p2}(i_{q\_ref} - i_q) + k_{i2}\int(i_{q\_ref} - i_q)dt \qquad (15)$$

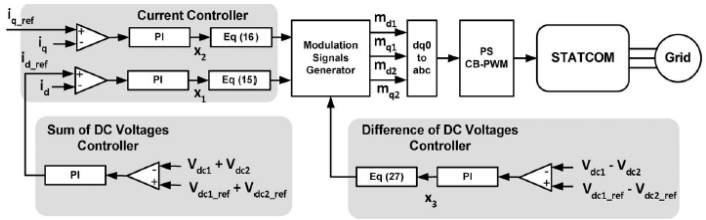

Fig-4 Controller Circuit of Statcom

B. Reactive Power Control

STATCOMs are commonly used either for transmission line voltage support or for reactive power compensation of load. For voltage support of the transmission line, the reactive current reference i_{q_ref} is controlled by the deviation of the transmission-line voltage from its nominal value. On the other hand, for load compensation operation, the reactive current reference i_{q_ref} is controlled by the deviation of source power factor from its required value. In both the aforementioned cases, i_{q_ref} will be supplied to the current controller by a higher level controller. The issues pertaining to the higher level controller are kept outside the purview of this paper.

C. DC Voltage Control

DC voltage controller should ensure that the two dc-link voltages *v*dc1 and *v*dc2 are regulated at their reference values. This problem is divided into two separate control objectives:

1) Sum of DC Voltages:

2) Difference of DC Voltages:

The sum of the voltages i.e.V_{dc1} and V_{dc2} increases the real power flow from grid to statcom and vice versa and the difference of voltages reflect the difference in power requirement between VSC-1 and VSC-2.

D. Generation of Modulation Signals

The current controller, shown in Fig. 4generates the signals for primary voltages $e_{d1} - e_{d2}$ and $e_{q1} - e_{q2}$. These are transformed to modulation signals as follows:

$$m_{d1}v_{dc1} - m_{d2}v_{dc2} = e_{d1} - e_{d2}$$

$$m_{q1}v_{dc1} - m_{q2}v_{dc2} = e_{q1} - e_{q2} \qquad (16)$$

V. Simulink Model Of Dual Converter

Simulation Result

Simulations have been performed to confirm the theoretical calculation of the overall efficiency and the current THD to verify the feasibility of the dual converter based STATCOM

Table – 1: Simulation Parameter

Parameter	Value
Power Rating	2.3KVA
Power Frequency	50 Hz
LV Side Voltages ea	107Vrms
Switching Frequency	900Hz
DC link Voltages Vdc1	282V
DC link Voltages Vdc2	106V
DC Link Capacitor,C	825uf
Leakage inductance ,L	2.1mH

Using above simulation parameters the simulation circuit is constructed and it is shown in fig.5and the subsystem of the circuit i.e the controller circuit is shown in fig-6 .

Asymmetric Dual Converter Based Statcom Circuit

The Statcom consist of two asymmetrical converter the input to the converter is the DC source and in output side we are connecting the transformer .The controller circuit is placed in between the converter and transformer .The simulation result of the DUAL converter is shown in fig-5

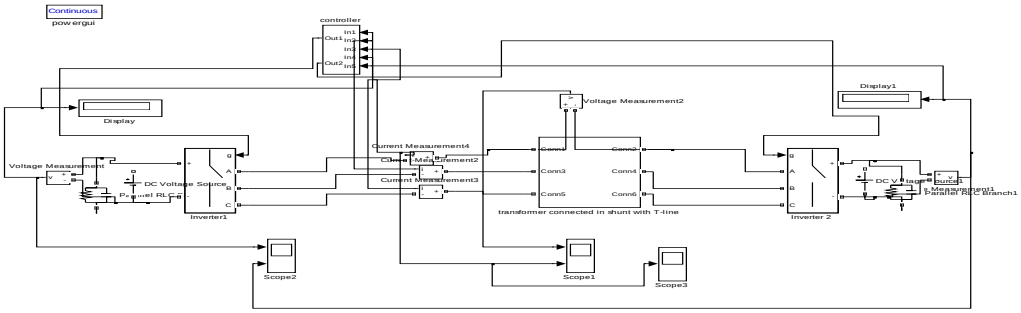

Fig-5 MATLAB/Simulink Model Circuit of asymmetric Dual converter base Statcom

PI Controller of the Dual Converter Based Statcom

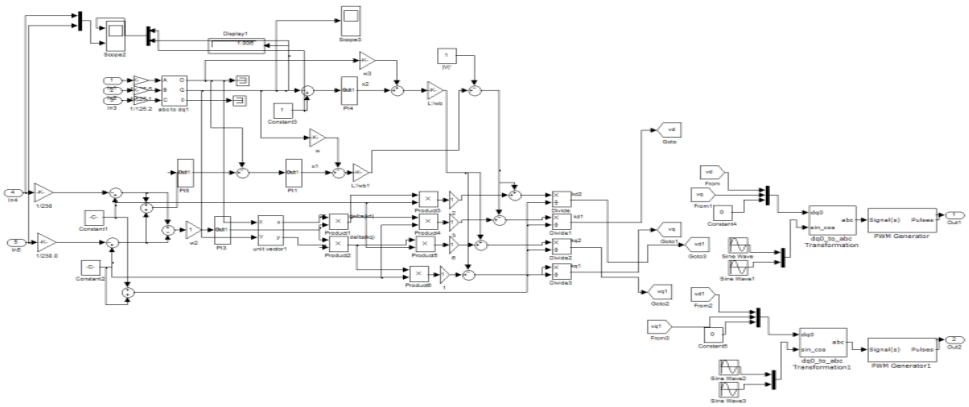

Fig-6 MATLAB/Simulink Model diagram of the controller

The output side voltage of the inverter which is five level and the maximum voltage is 800v.

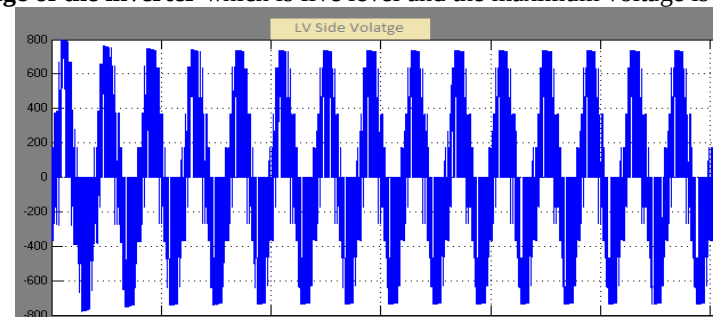

Fig-7 Shows the voltage waveform of LV side

Similarly the input side current of the transformer is shown in fig -8

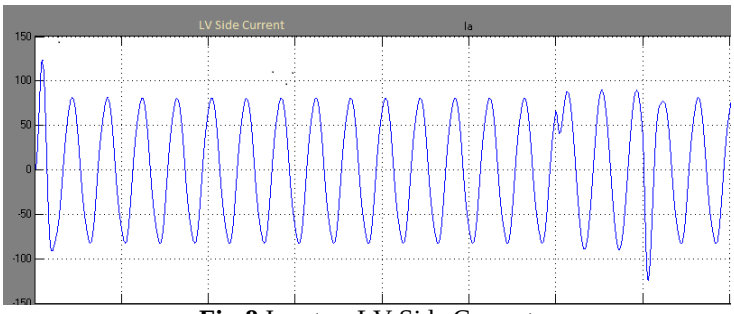

Fig-8 Input or LV Side Current

THD of the proposed asymmetric converter

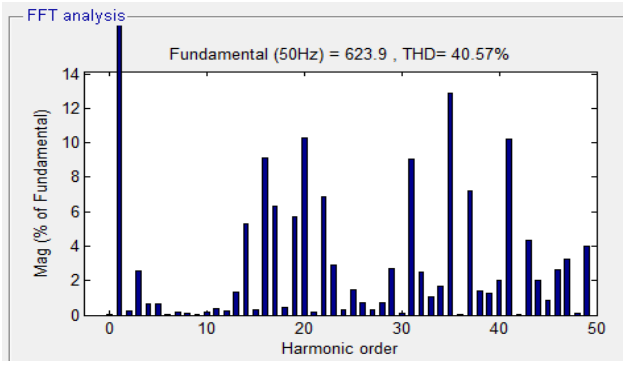

Fig-9 THD of the 4-level converter

NINE-LEVEL DIODE CLAMPED DUAL CONVERTER BASED STATCOM DIAGRAM

Diode Clamped multilevel Inverter

The diode clamped multilevel converter shown in Fig. 10 uses a series string of capacitors to divide the dc side voltage into several levels. Normally an N-level diode-clamped multilevel inverter has 2(N−1)main switches and2(N−1)main diodes per phase. The switches of each phase leg are connected via power diodes to the different voltage level points set by the dc capacitors. When operating, two adjacent switches (for a three-level converter) in each phase leg are ON to provide a respective voltage level; therefore, the line voltage waveforms are synthesized by different combinations of switches.

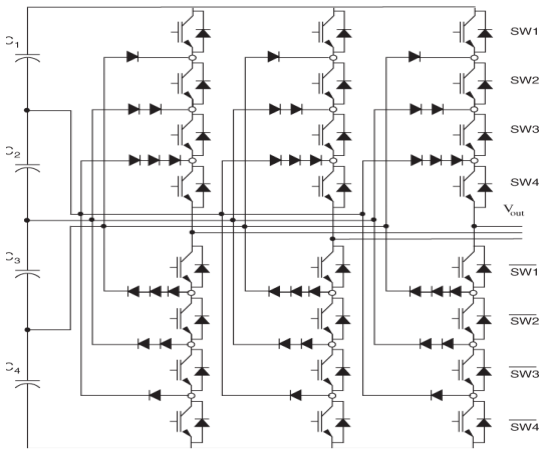

Fig-10 Three phase 9-level DCMLI circuit

The main features of DCMLI are

- When the number of level increases the harmonics content is low and it avoids the need for filter.
- Inverter efficiencies is high because all devices are switched at fundamental frequencies
- The control method is simple.

Table-II

Nine Level $V_1 > V_2$	Five Level $V_1 = V_2 = V$
$V_1 + V_2$	$2V$
V_1	V
V_2	V
$V_1 - V_2$	0
0	0
$V_2 - V_1$	0
$-V_2$	$-V$
$-V_1$	$-V$
$-V_1 - V_2$	$-2V$

Nine-level verses Five-level Converter

By careful selection of the switching voltages, the nine-level converter can provide superior harmonic performance. A comparison of the five-level output waveform to a nine-level waveform is shown in Table II. The corresponding nine-level output waveform is shown in Fig. 11

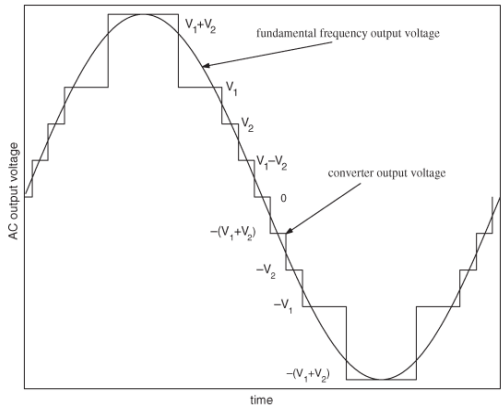

Fig-11 Nine-level Voltage wave form

Diode-clamped converters are used less frequently in industrial applications than cascaded converters due to the potential for charge imbalance of the capacitors. However, recent advances in charge-balancing methods have made the diode clamped converter more attractive [8]–[9]. The two most common approaches for charge balancing are to introduce an external balancing circuit or to use space-vector modulation[5], [6]. The primary drawback to the cascaded topology is that each leg requires an isolated voltage source for active-power conversion. Due to the strict requirement that each dc source must be electrically isolated. So diode clamped inverters are used in that condition.

MATLAB/Simulink Model of nine-level dual converter based STATCOM

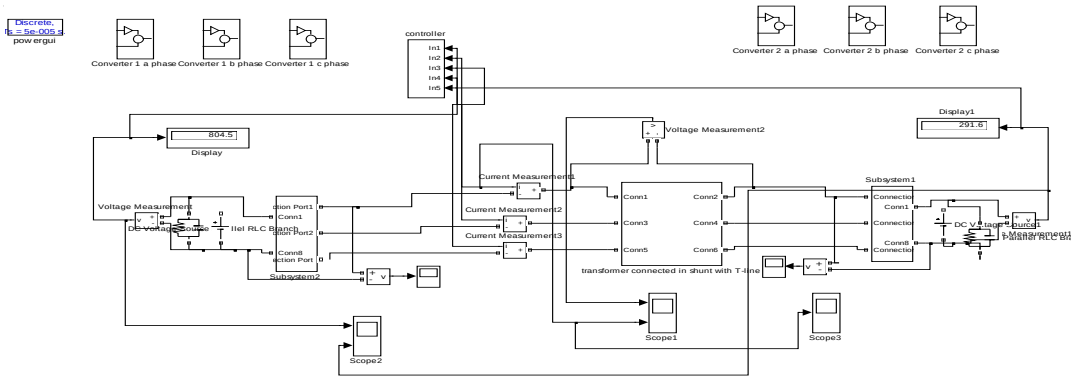

Fig-12 MATLAB/Simulink Model of nine-level dual converter based STATCOM

Simulated Result of 9-level output wave form

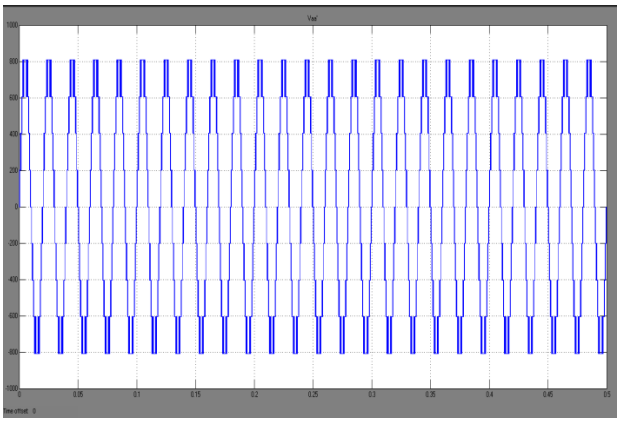

Fig-13 Shows the output waveform of 9-level DCMLI based Statcom

THD of the Nine-level Diode clamped inverter

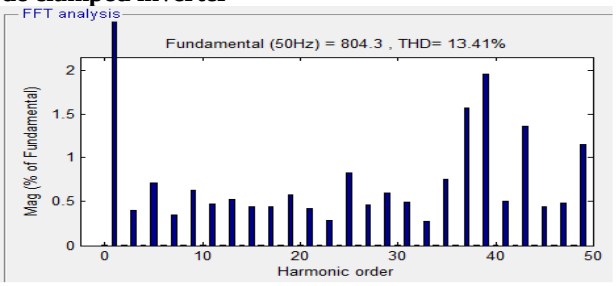

Fig-14 Shows the THD of the DCMLI

VI. Conclusion

This paper has presented a of asymmetric dual converter based STATCOM. The use of lesser component and the reduced capacitance are the enhancing features of the scheme over the other converter. A Nine-level Diode clamped Multilevel Inverter controller has been proposed to regulate the dc-link voltages of the two converters by drawing requisite amount of real power from the utility and by differentially distributing them between the two converters. The circuit operation and controller is developed in MATLAB/SIMULINK. The main advantage of the proposed topology is that the THD is reduced. Many other parameters can be modeled and investigated using the same model which all left for future research. This system is also applied to various other resources of VSC.

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