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BCH Decoder Implemented On CMOS/Nano Device Digital Memories for Fault Tolerance Systems Design

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ABSTRACT— *In this paper present two fault-tolerance systems design approaches. The fault tolerance value design for CMOS/Nano device digital memories. Two faults identified that ones for intermittent fault another transient faults. These two approaches share several key features, including the use of a group of Bose-Chaudhuri- Hocquenghem (BCH) codes for both intermittent fault tolerance and transient fault tolerance, and integration of BCH code selection and dynamic logical-to-physical address mapping. BCH codes invented in 1960s are powerful class of multiple error correction codes with well defined mathematical properties, used to correct multiple random error patterns. The mathematical properties within which BCH codes are defined are the Galois Field or Finite Field Theory. Thus, a new model of BCH decoder is proposed to reduce the area and simplify the computational scheduling of both syndrome and chien search blocks without parallelism leading to high throughput. For implementation Spartan 3E FPGA processor is used with VHDL and the simulation & synthesis are performed using Xilinx ISE 12.1.*

Keywords*—Bose Chaudhuri Hocquenghem (BCH)codes, complementary metal oxide semiconductor(CMOS), Breklamp Massey Algorithm(BMA),very large scale integration circuits(VLSI), Field programmable gate array(FPGA).*

I. INTRODUCTION

This past few years experienced spectacular advances in the fabrication and manipulation of molecular and other nano scale device [1]. Although these new devices show significant future promise to sustain Moore's law beyond the CMOS scaling limit, there is a growing consensus [2], that at least in the short term, they cannot completely replace CMOS technology. As a result, there is a substantial demand to explore the opportunities for CMOS and molecular/nanotechnologies to enhance and complement each other.

This naturally leads to a paradigm of hybrid CMOS/nano device nano electronics, where any of array of nano wire crossbars, with wires connected by simple nano devices at each cross point site on the top of a bulk information processing and/or storage, while the CMOS circuit may some perform testing and fault tolerance, global interconnect, and some other critical functions. It is almost evident that, compared with the current CMOS technology, any emerging nano devices will have (much) worse reliability characteristics (such at the probabilities of permanent defect and transient fault). There are four technologies used in the domain.

CMOS TECHNOLOGY
NANO TECHNOLOGY
BCH TECHNOLBMA
BMA TECHNOLOGY

Hence, fault tolerances have been well recognized as one of the biggest challenges in the emerging hybrid nano electronics.

II. BCH DECODE

This work concerns the fault-tolerant system design for hybrid nano electronic digital memories. Conventionally, defect and transient faults in CMOS digital memories are treated separately, i.e., defects are compensated by using spare rows, columns, and/or words to repair (i.e., replace) the defective ones, while transient faults are compensated by error correcting codes (ECC) such Hamming and Bose-Chaudhuri-Hocquenghem (BCH) codes. The Bose-Chaudhuri- Hocquenghem (BCH) codes form a large class of powerful random error-correcting cyclic codes. This class of codes is a remarkable generalization of the Hamming codes for multiple-error correction. For any positive integer's m ($m \geq 3$) and t ($t < 2^m 1$), there exists a binary BCH code with the following parameters:

Block length: $n=2^m-1$
Number of parity check digits: $n- k \leq mt$.
Minimum distance: $d_{min} \geq 2t$

Clearly, this code is capable of correcting any combination of t or fewer errors in a block of $n = 2^m-1$ digits. We call this code a t- error-correcting BCH code. The generator polynomial of this code is specified in terms of its roots from the Galois field GF (2^m) using binary BCH code decoder structure figure(1). BCH decoding stepping method. The basic idea of the BCH code decoder is to detect an erroneous sequence with few words, who summoned the received data, gives rise to a valid code word. Several steps are required for decoding these codes:

- Calculation of syndrome.
- Calculation of polynomials error localization and amplitude.
- Calculation of roots and evaluation of two polynomials.
- Sum of the polynomial consists of the polynomial and to reconstruct the received information.
- Start without error.

This can be summed in the upcoming figure for easier conception of the VHDL source-code that we will be using in the conception of our BCH decoder. The BCH codes are implemented as cyclic codes, that is, the digital logic implementing the encoding and decoding algorithms is organized into shift-register circuits that mimic the cyclic shifts and polynomial arithmetic required in the description of cyclic codes. Using the properties of cyclic codes, the remainder can be obtained in a linear stage shift register with feedback connections corresponding to the coefficients of the generator polynomial as shown in the following figure(2),

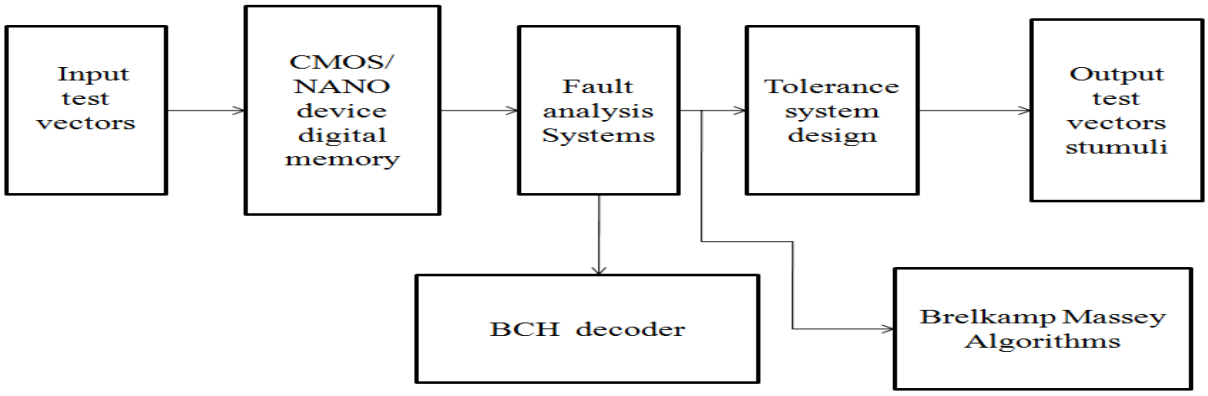

Figure.1 Block diagram of Digital circuit for BCH decoder

Where:
R(x): received code word
S(x): the calculated syndrome
σ(x): The error locating polynomial
C(x): Codeword after decoding.

III. BMA (BERKLAMP MASSEY ALGORITMS)

In this paper we used the algorithm of BERKLAMP-MASSEY from the fact that it was specially made for the decoding of this type of codes. The four technologies: The Berlekamp–Massey algorithm is an algorithm that will find the shortest linear feedback shift register (LFSR) for a given binary output sequence. The algorithm will also find the minimal polynomial of a linearly recurrent sequence in an arbitrary field. The field requirement means that the Berlekamp–Massey algorithm requires all non-zero elements to have a multiplicative inverse.[1] Reeds and Sloane offer an extension to handle a ring. James Massey recognized its application to linear feedback shift registers and simplified the algorithm. The Massey termed the algorithm the LFSR Synthesis Algorithm (Berlekamp Iterative Algorithm), but it is now known as the Berlekamp–Massey algorithm. Due to more complicated initial states, the number of iterations is decreased by one. In practice, this causes only a slight increase in the hardware requirements but the BMA calculation time is significantly reduced. The error location polynomial $\sigma(x)$ is obtained in the C registers after $t-1$ iterations. In some applications it may be beneficial to implement the BMA without inversion.

IV. IMPLEMENTATION OF BCH DECODER

(i) GALOIS FIELD GF (2^m)

Because of their strong random error correction capability, binary BCH codes[3] are among the best ECC candidates for realizing fault tolerance in hybrid nano electronic digital memories where the faults(both defects and transient faults) are most likely random and statistically independent. Binary BCH code construction and encoding/decoding are based on binary Galois fields.

A binary Galois field with degree of m is represented as GF (2^m). For any $m \geq 3$ and $t \leq 2^{m-1}$, there exists a primitive binary BCH code over GF (2^m), denoted as C^m (t), that has the code length $n=2^m-1$ and information bit length $k \geq 2^m-m.t$ and can correct up to (or slightly more than) t error. For most values of t, $C^m(t+1)$ requires m more redundant bits than $C^m(t)$.

A primitive t-error-correcting (n, k, t) BCH code can be shortened (i.e., eliminate a certain number, say s, of information bits) to construct a t-error-correcting (n-s, k-s, t) BCH code with less information bits and code length but the same redundancy [3]. Although BCH encoding is very simple and only involves a Galois field polynomial multiplication, BCH code decoding algorithms may lead to (slightly) different decoding computational result, (n, k, t) binary BCH code under GF(2^m) , the product of the decoder silicon area and decoding latency is approximately proportional to $n .t . m^2$.

Moreover, a group of binary BCH codes under the same GF (2^m) can share the same hardware encoder and decoder that are designed to accommodate the maximum code length, maximum information bit length, and maximum number of correctable errors among all the codes within the group. For a detailed discussion on BCH codes and their encoding/decoding, readers are referred to [4] and [5]. In order to realize satisfactory intermittent tolerance efficiency, the repair-only approach requires very low defect densities that can be readily met by current CMOS technology.

V. NANO TECHNOLOGY AND STRUCTURES

The **Nanotechnology** ("nanotech") is the manipulation of matter on an atomic, molecular, and supramolecular scale. The earliest, widespread description of nanotechnology referred to the particular technological goal of precisely manipulating atoms and molecules for fabrication of macro scale products, also now referred to as molecular nanotechnology. A more generalized description of nanotechnology was subsequently established by the National Nanotechnology Initiative, which defines nanotechnology as the manipulation of matter with at least one dimension sized from 1 to 100 nanometers.

This definition reflects the fact that quantum mechanical effects are important at this quantum-realm scale, and so the definition shifted from a particular technological goal to a research category inclusive of all types of research and technologies that deal with the special properties of matter that occur below the given size threshold. It is therefore common to see the plural form "nanotechnologies" as well as "nano scale technologies" to refer to the broad range of research and applications whose common trait is size.

More importantly, realization of fault tolerance and transient fault tolerance in hybrid nano electronic memory will incur area, energy and operational latency overhead in CMOS domain, e.g., the overhead incurred by the implementation of ECC decoder and reliable storage of certain nano device memory configuration information in CMOS memory in figure 2.

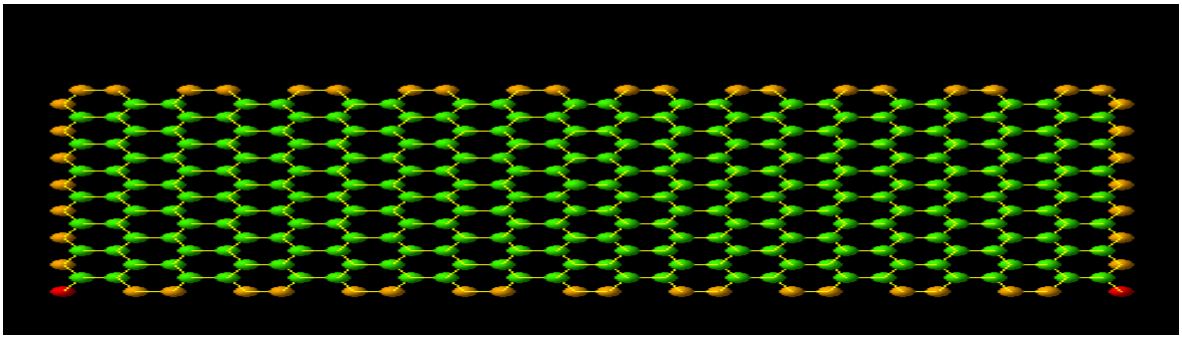

Figure. 2 Nano device structure

Such overhead in CMOS domain must be taken into account when investigating and evaluating hybrid nano electronic digital memory fault-tolerant system design solution. Defect tolerances in hybrid nanoelectronic digital memory have been addressed [6]. In the authors analysed the effectiveness of integrating Hamming codes with spare tow/column repair only defect tolerance. The ECC-only defect tolerance has been used to estimate the hybrid nano electronic memory storage capacity. This paper presents in hybrid nano electronic digital memory fault-tolerant system design approaches using strong BCH codes, and evaluates the BCH coding system implementation overhead in CMOS domain based on practical IC design. We understand that, at this early stage of nano electronic when few preliminary experimental data under laboratory environments have been ever reported, there is a large uncertainty of the defect and transient fault statistical characteristics (such as their probabilities and temporal/spatial variations) in the future real-life hybrid CMOS/nano device digital memories in table 1.

Table :1

Port Name	Type	Description
Data	Input	16-bit data input to digital memory
Clock	Input	Clock
read address	Input	8-bit read address input
write address	Input	8-bit write address input
We	Input	Write enable input
Q	Output	16-bit data output of digital memory

Table.1 Binary memory port pin allocation

Therefore, instead of attempting to provide a definite and complete fault-tolerant system design solution, this work mainly concerns the feasibility and effectiveness of realizing memory fault tolerance under as-worse-as-possible scenarios. In particular, we are interested in the fault-tolerant strategies with two features: They should be high as possible of the defect probabilities and transient fault rates and 2) they can automatically adapt to the variations of the defect statistics in digital memories (i.e., the on-chip fault-tolerant system can automatically provide just enough defect tolerance capability for a wide range of defect[7].

VI. BCH DECODER IMPLEMENTED FPGA SPARTAN 3E KIT

In nano device memory, due to the high defect probabilities and their possibly large temporal/spatial variations, different physical memory portions may have (largely) different physical memory cell hence demand (largely) different error correcting capability. Therefore, other than using a single BCH code, we propose to use a group of BCH codes in the group should be constructed under the same binary Galois field. A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC). (Circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare.

The FPGA Spartan 3E starter board in order to display the results on the LCD screen that exists on the board. It has many others blocs distend to different areas of use in the world of micro-technology. The FPGA Spartan 3E starter is shown in the following figure 3.

Figure.3 Spartan FPGA Starter Kit

In this work, to demonstrate and evaluate the proposed fault- tolerance design approaches, we constructed four BCH code groups as list [8]. While implementation of syndrome computational and Chine search blocks are straightforward, the realization of error locator calculation is nontrivial and several algorithms have been proposed in the regard. In this work, we use the inversion – free Brelekamp – Massey to realize the error locator calculation. To minimize the decoders are fully serial, i.e., it receives 1 – bit input and generates 1-bit output per clock cycle [9].

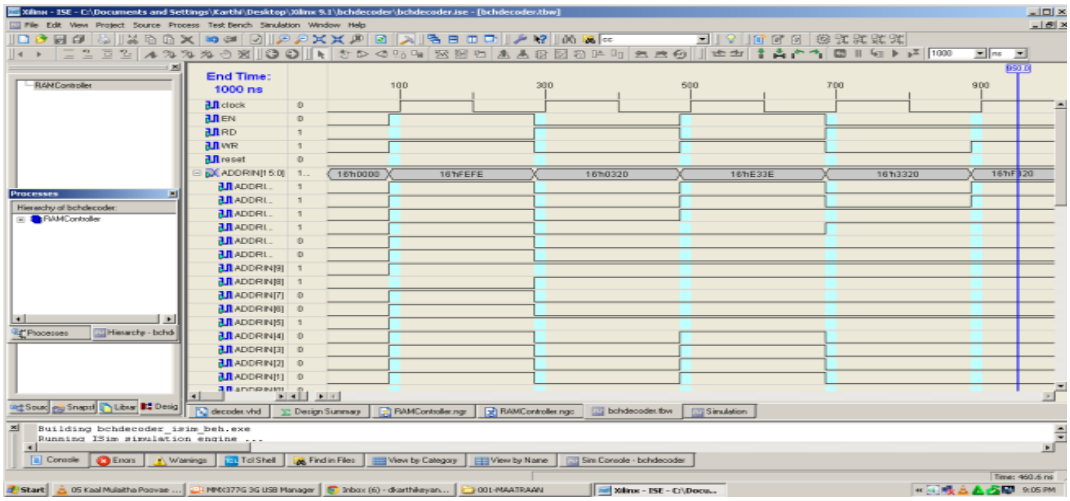

Figure. 4 Binary BCH code and test bench wave form

VII. PROPOSED FAULT – TOLERANT DESIGN APPROACHES

In this work, we assume the following fault model for nano device memory. In terms of defect, we only consider static defects of nano wires and nano device memory cells. We assume a defective nano wire (irrelevant to defect type) will make all the connected nano device memory cells un functional. A memory cell may be subject to open or short two orthogonal nano wire defects. An open memory cell defect does not affect the operation of any other are memory cells and any nano wires.

The Bit defect probability p_{bit} that represents the probability of the open memory cell defect. Given the BCH code group and memory defect map, a fault-tolerant system should determine.

1) Bit user data block and 2) how to physically map each BCH decoded data block onto the nanodevice memory cell.

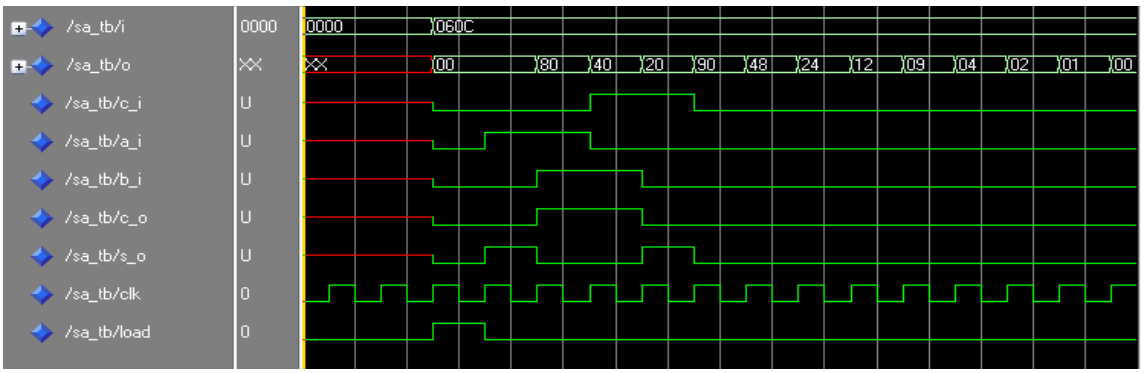

Figure. 5 simulation wave form fault analysis.

(i) Two Level Hierarchical Fault Tolerance

The basic idea of this design approach can be described as follows: we partition each nano device memory cell array into a certain number of memory cell segments; each segment contains consecutive memory cells and can store one BCH codeword that provide just enough coding redundancy to compensate all the defects in present segment and ensure a target block error rate under a given transient fault rate in figure (4). This first approach is simple and works well under relatively low and modest bit probabilities and/or transient fault rate in figure 5&6.

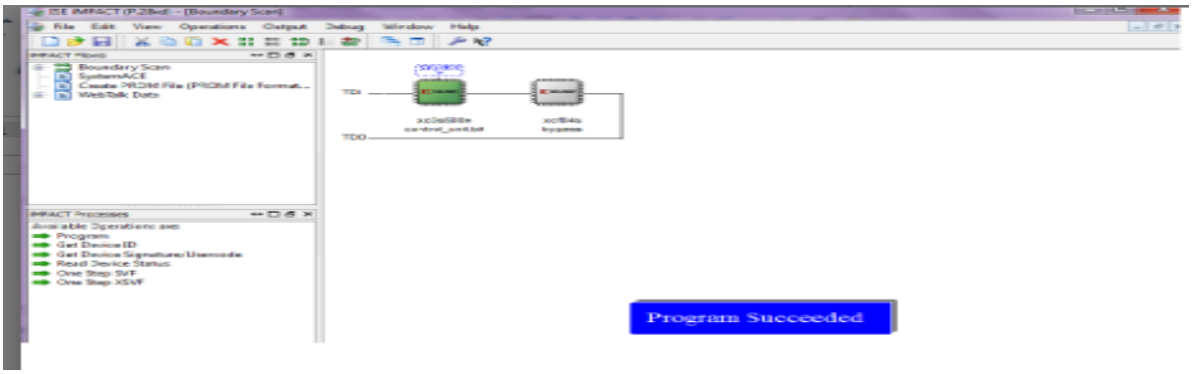

Figure. 6 Programming Operations Complete.

(ii) Three- Level Hierarchical Fault Tolerance

In the above two- level hierarchical design approach, we always attempt to locate a continuous memory cell segment to store each coded data block. Hence, with high bit defect probabilities, the total number of defective memory cells within a segment may accumulate very quickly and exceed the maximum error correcting capability in figure 7.

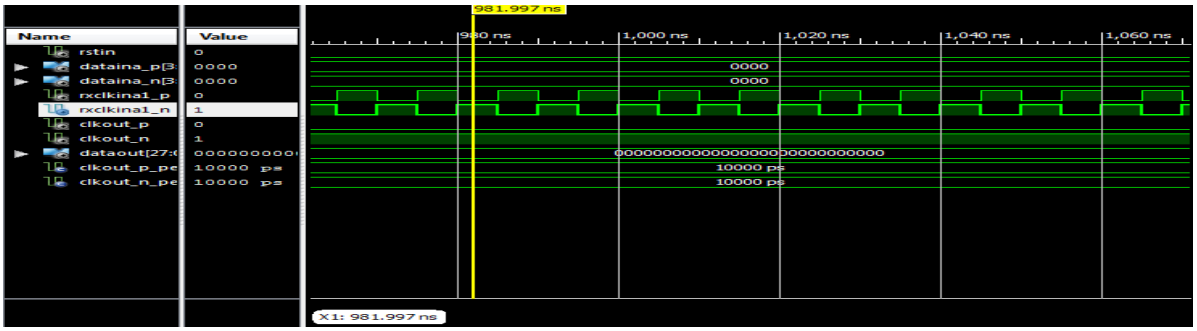

Figure. 7 Simulation result output waveform of bch decoder.

VIII.CONCLUTION

A binary BCH decoder consists of three computational blocks and one first in first out (FIFO) buffer. To accommodate the high intermittent probabilities and transient fault rates, the developed approaches have several key features that have not been used in conventional digital memories, including the use of a group of BCH codes for both intermittent tolerance and transient fault tolerance, and integration of BCH codes selection and dynamic logical-to-physical address mapping. These two fault-tolerance design approaches seek different tradeoffs among the achievable storage capacity, robustness to defect statistics variations, implementation complexity, and operational latency and CMOS storage overhead. Simulation results demonstrated that the developed approaches can achieve good storage capacity, while taking into account of the storage overhead in CMOS domain, under high intermittent probabilities and transient fault rate, and can readily adapt to large defect statistics variations. Also design of BCH decoder successfully implemented on Spartan 3E FPGA hardware. The Synthesis was successfully done by using the RTL compiler, power and area is estimated technology.

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