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Design Of Electrocardiogram (ECG Or EKG) System On FPGA

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Abstract— *The aim of this paper is to design and implement an advanced Electrocardiogram (ECG) signal monitoring and analysis system design using FPGA. An electrocardiogram, also called an ECG or EKG, is a simple, painless test that records the heart's electrical activity. The main Tasks in ECG signal analysis are the detection of how fast heart is beating, whether the rhythm of your heartbeat is steady or irregular and the strength and timing of electrical signals as they pass through each part of your heart. An algorithm based on wavelet transforms which uses the linear quadrature mirror filter (QMF) B-spline wavelet for the detection of QRS complex is developed and implemented on FPGA. The proposed FPGA based Electrocardiogram system can operate with high performance, Time to Market, Low cost, high reliability, long-term to Maintenance, and maximum throughput of 52.67 MSamples/sec. Thus the system can work on both online and offline at maximum throughput. The system is* ***designed and implemented using*** *Verilog language* ***and Xilinx FPGA respectively.***

Keywords— *FPGA, Electrocardiogram (ECG), FIR, Xilinx, Algorithm a Trous, P and T waves.*

I. INTRODUCTION

The electrocardiogram or ECG (sometimes called EKG) is today used worldwide as a relatively simple way of diagnosing heart conditions. An electrocardiogram is a recording of the small electric waves being generated during heart activity. The main tasks in ECG signal analysis are the detection of QRS complex and the estimation of instantaneous heart rate. They are many hardware implementation approaches to ECG (or EKG) monitoring systems. They are micro-controller based ECG, DSP based medical development kits which include Electrocardiogram and Pulse oxiometere.It is limited by performance by clock rate. Compared to microcontroller, DSP based medical kit and ASIC, FPGAs are low cost and reconfigurable property, have a low time to market.

II. ELECTROCARDIOGRAM

Electrocardiogram ECG signal has been widely used for heart diagnoses .In this paper, we presents the design of Heart Arrhythmias Detector using Verilog HDL based on been mapped on small commercially available FPGAs Field Programmable Gate Arrays. Majority of the deaths occurs before emergency services can step in to intervene. In this research work, we have implemented QRS detection device developed by Ahlstrom and Tompkins in Verilog HDL. The generated source has been simulated for validation and tested on software Verilogger Pro6.5.[11] We have collected data from MIT-BIH Arrhythmia Database for test of proposed digital system and this data have given MIT-BIH data as an input of our proposed device using test bench software. We have compared our device output with MATLAB output and calculating the error percentage and got desire research key point of RR interval between the peaks of QRS signal. The proposed system also investigated with different database of MIT-BIH for detect different heart Arrhythmias and proposed device give output exactly same according to our QRS detection algorithm.The spikes and dips in the line tracings are called waves. See a picture of the ECG **Fig.1**

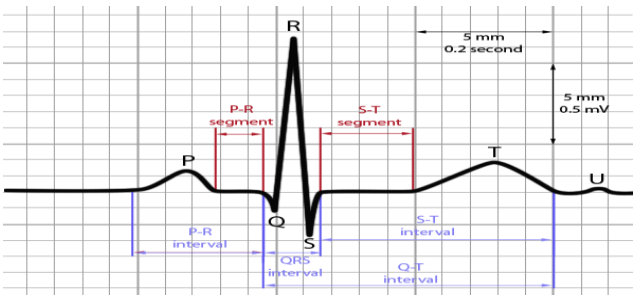


Fig.1 ECG signal characteristics

- ✓ The P wave represents the atrial contractions.
- ✓ QRS complex represents the ventricular contractions. The R peak indicates a heartbeat.

- ✓ The T wave is the last common wave in an ECG. This electrical signal is produced when the ventricles are repolarizing.
- ✓ The letters used in the ECG signal description do not have abbreviations in medical terminology.

The heart is a muscular pump made up of four chambers. The two upper chambers are called atria, and the two lower chambers are called ventricles. A natural electrical system causes the heart muscle to contract and pump blood through the heart to the lungs and the rest of the body.

III. EXISTING METHOD

The earlier method of ECG signal analysis was based on time domain method and are micro-controller based ECG, DSP based medical development kits but this is not always sufficient to study all the features of ECG signals. So, the frequency representation of a signal is required. To accomplish this, FFT (Fast Fourier Transform) technique is applied using Direction-Adaptive Discrete Wavelet Transform in FPGA. But the unavoidable limitation of this FFT is that the technique failed to provide the information regarding the exact location of frequency Components in time. As the frequency content of the ECG Signal Analysis Using Discrete Wavelet Transforms ECG varies in time, the need for an accurate description of the ECG frequency contents according to their location in time is essential. This justifies the use of time frequency representation in quantitative electro cardiology.[12]

IV. PROPOSED METHOD

To overcome the draw backs of FFT, the immediate tool available for this purpose is the Short Term Fourier Transform (STFT). But the major draw-back of this STFT is that its time frequency precision is not optimal. Hence we opt a more suitable technique to overcome this drawback. Among the various time frequency transformations the wavelet transformation is found to be simple and more valuable. The wavelet transformation is based on a set of analyzing wavelets allowing the decomposition of ECG signal in a set of coefficients. Each analyzing wavelet has its own time duration, time location and frequency band. The Wavelet coefficient resulting from the wavelet transformation corresponds to a measurement of the ECG components in this time segment and frequency band.

V. DISTRIBUTIVE ARITHMETIC BASED 2D DWT/IDWT ARCHITECTURE

In this section, we first outline how to perform multiplication by using memory based architecture. Following this, we briefly explain architecture for DWT filter bank. Using this we show complete design for block based DWT. The memory based approach provides an efficient way to replace multipliers by small ROM tables such that the DWT filter can attain high computing speeds with a small silicon area as shown in Figure 3. Traditionally, multiplication is performed using logic elements such as adders, registers etc. However, multiplication of two n-bit input variables can be performed by a ROM table of size of 22n entries. Each entry stores the pre-computed result of a multiplication. The speed of the ROM lookup table is faster than that of hardware multiplication if the look-up table is stored in the on-chip memory. In DWT, one of the input variables in the multiplier can be fixed. Therefore, a multiplier can be realized by 2n entries of ROM. Distributed arithmetic implementation of the Daubechies 8-tap wavelet FIR filter consists of an LUT, a cascade of shift registers and a scaling accumulator [12].

VI. DISCRETE WAVELET TRANSFORM (DWT)

Discrete Wavelet Transform (DWT) has been used in the last few years in applications of signal processing like denoising, compression and coding. Methods for both offline and online mode have been proposed. In the first, the information is processed frame-by-frame; in the second, it is processed sample-by-sample. An algorithm presented in [7] gives a rapid decomposition of the discrete wavelet transform. Succinctly, it expresses the Wavelet coefficients C_{ik} and d_{ik} at a resolution j with two simple digital filtering equations :

$$c_{jk} = \sum_{n} h_{n-2k}\ c_{j-1,n} \qquad (1)$$

$$d_{jk} = \sum_{n} g_{n-2k}\ c_{j-1,n} \qquad (2)$$

In these equations, h_n and g_n are the coefficients of the filters H and G , which are related to the scaling function and wavelet function.H is a low-pass filter, whereas G is a high-pass filter. If we consider separable filters, the previous analysis can be extended to two-dimensional spaces. In that context, image processing consists of successive filtering along two perpendicular axes. For example, we can first consider filtering along the image rows, then along the columns. The corresponding decomposition is illustrated by Figure 2.

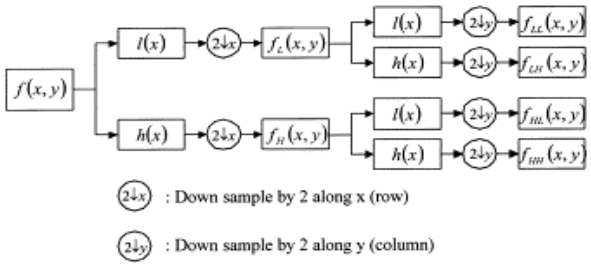


Figure 2. Discrete Wavelet Transform Archetcture

VII. DIRECTION-ADAPTIVE DISCRETE WAVELET TRANSFORM (DA-DWT) ARCHITECTURE IMPLEMENTED ON FPGA:

Algorithm -1
BEGIN
Step 1: Loading of original signal
Step 2: Detect QRS complex in every heart beat
Step 3: Cut and align the signal beat by beat
Prior to 2-D transformation
Step 4: Segmentation into NXN blocks (to
Construct 2-D array from 1-D array)
Step 5: Apply DWT to get the transformed Information using by DA-DWT architecture.
Step 6: Find the transformed coefficients
Step 7: Apply 2-D transform coding to achieve the essential compression.
Step 8: Displaying the result
END
Algorithm- 2
Step 1.The samples of input ECG signal are divided into even and odd in the first stage.
Step 2.Using shift register, upper four shift register store MSB bits and lower four shift register stores the LSB bits.
Step 3.Clock cycles are required to load the shift register contents. After clock cycle, the control logic configures the shift register as serial in parallel out, forming the address for the LUT.
Step 4.Partial products stored in the LUT are read simultaneously front all the four LUTs.
Step 5.Accumulated with previous values available across the shift register in the output stage.
Step 6.The output stage consisting of adders, accumulators and shift registers are used to accumulate the LUT contents and compute the
DWT output.
Distributed Arithmetic replaces multiplications by ROM look-up table (LUT) so that DWT filter can achieve high computing speed with small area by 82% in hardware design.

7.3.Wavelet Analysis

The wavelet analysis of ECG signal is performed using MATLAB software. MATLAB is a high performance and high Reliable interactive system which allows to solve many technical computing problems. The MATLAB software package is provided with wavelet tool box. It is a collection of functions built on the MATLAB technical computing environment. It provides tools for the analysis and synthesis of signals and images using wavelets and wavelet packets within the MATLAB domain.

7.4.ADC MODULE

High-speed analog to digital converters (A/D) and large fieldprogrammable gate arrays (FPGA) have allowed designers to design compact solutions that were unthinkable a few years ago.FPGAs are well suited for serial Analog to Digital converters. This is mainly because serial interface consumes less communication lines while the FPGA is fast enough to accommodate the high speed serial data. The DCS7476MSPS is a high speed, low power, 14-bit A/D converter. A/D converter is a high speed serial interface that interfaces easily to FPGAs. The A/D interface adapter (AD1_PMOD) is implemented within the FPGA.Inside the FPGA, this adapter facilitates parallel data acquisition. Sampling is initiated at the rising edge of a clock applied at the line sample. The timing diagram of the communication protocol obtained with Modelsim is illustrated.[1]

Figure-3 analog to digital converters (A/D) FPGA

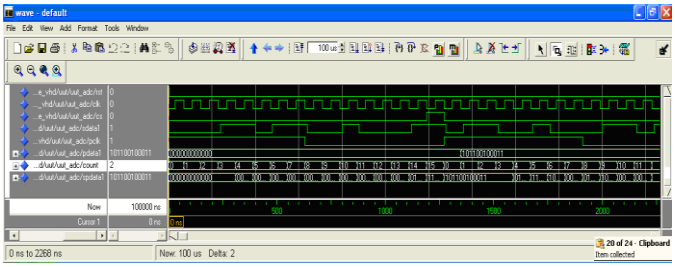


Figure-4: Simulation analog to digital converters (A/D) Interface

VIII. SPARTAIN 3E FPGA ARCHITECTURE

The Spartan product is a cost reduced high volume FPGA. Most Spartan devices are a close relative to another Xilinx product.The Spartan-3E FPGA family offers the low cost and platform features you're looking for,making it ideal for gate-centric programmable logic designs.Sparatan-3E is the seventh family in the groundbreaking low-cost Spartan Series and the third Xilinx family manufactured with advanced 90nm process technology.Spartan-3E FPGAs deliver up to 1.6 million system gates, up to 376 I/Os, and a versatile platform FPGA architecture with the lowest cost per-logic in the industry.This combination of state-of-theart low-cost manufacturing and cost-efficient architecture provides unprecedented price points and value.The features and capabilities of the Spartan-3E family are optimized for high-volume and low-cost applications and the Xilinx supply chain is ready to fulfill your production requirements.There are several Spartan FPGA families:

–Spartan-II, Spartan-IIE
–Spartan-3 Generation
•Spartan-3 (high density and pin count)
•Spartan-3E (optimized for logic cost)
•Spartan-3A (optimized for pin cost)
•Spartan-3AN (enhanced with non-volatile flash)
•Spartan-3ADSP (enhanced for signal processing.
The FPGA archetecture, Spartain-3E shown in below figure

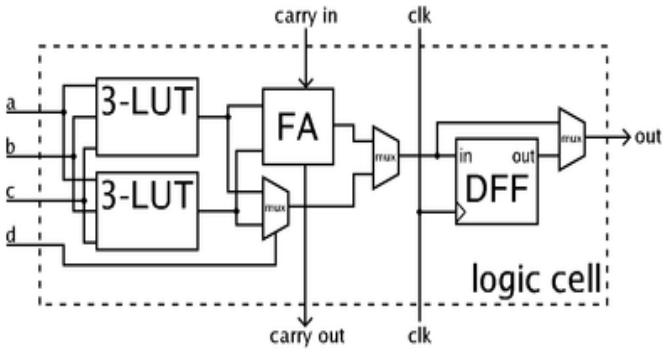


Figure.5: FPGA architecture.

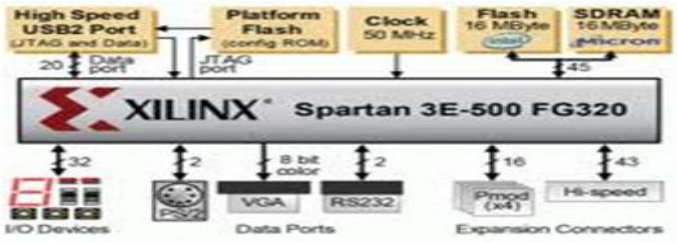


FIGURE6: FPGA ARCHITECTURE SPARTAIN 3E

I X . PERFORMANCES

The simulation was achieved with the XC4000E Xilinx family and showed correct results at a rate of 75 ns per output.Since the processing rate is dissociated from the acquisition and the restitution rate, the delay needed for the whole treatment depends on the size of the images to be processed, sent on the video bus. It is shown below for a few image sizes, with regard to the video rate (25 images/s), for a 3 level decomposition:

Image size	processing rate
581x763	88 ms 1 image / 3
512x512	51,6 ms 1 image / 2
256x256	12,9 ms video rate

X. IMPLEMENTATION RESULTS

A. **Timing Summary:**

Minimum period: 1.537ns

Maximum Frequency: 650.576MHz

Maximum output required time after clock: 3.924ns

Maximum combinational path delay: No path found

B.Power Report

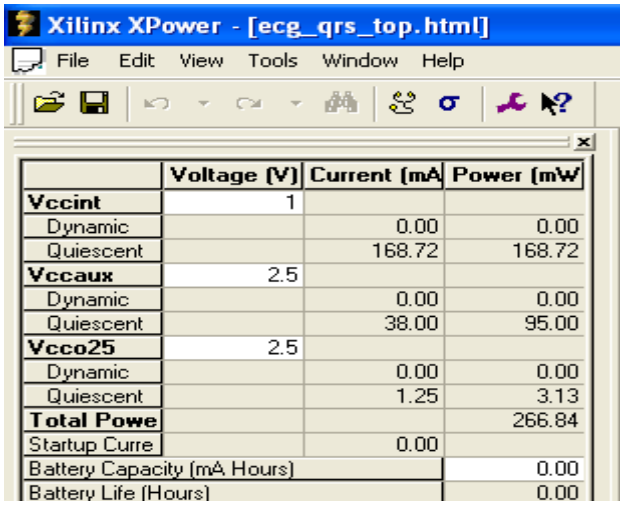
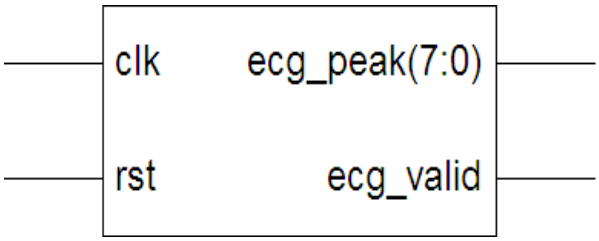


Figure 7: FPGA Synthesis Snapshot



XI. CONCLUSIONS

I Have Reported A Successful Development Of A Real-Time Ecg Monitoring System Using Discrete Wavelet Method Based On Fpga With Low Power.Ecg Monitor System To Collect, Store, Playback, Wireless Transmission Can Be Integrated Into A Fpga Chip, So That Greatly Reducing The Development Of Analog Circuits, Reducing Development Costs And Research And Design Cycle, Fpgas Are Low Cost And Reconfigurable Property, Have A Low Time To Market.The Ability To Automate The Fpga Design Process Saves Time And Increases Productivity. The Ise Software And The Quartus Ii Software Provide The Tools Necessary To Automate Your Fpga Design Flow.

XII. FUTURE ENHANCEMENT

This project shows how the heart rate was calculated by implementing ECG on the FPGA. As of now, the user interface module only shows the calculated heart beats per minute. A visual interface that can show the ECG waveform as a running graph can be very useful for diagnosing any abnormalities with the heart.Also, the project is implemented using ECG signals produced by a simulator. When working with an electrical signal coming directly from a person's heart, there will be substantial noise. In such a case, signal processing is a huge challenge since the actual signal value has very small amplitude. There are several other factors that impact accuracy like the pacemakers or the interference from the power supply. Obtaining a clean ECG signal, free of all noise without losing any important information is still a challenge in the medical domain.

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