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Analysis of Write Power Consumption for Single Gate and Dual Gate MOS Based SRAM

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Abstract:*In this paper the target is to study the write power of SRAM cell with dual-gate MOS.Earlier designed memories using single gate MOS faced the problem related with stray capacitance and leakage current which increase the write power dissipation with the shrinking MOS feature and the requirement of Low-power devices.CMOS scaling causes in low V_t(Threshold Voltage) and reduce oxide thickness.Reduction in high thickness at high bias voltage forced the electrons to tunnel through the gate.The proposed dual gate MOS cell present that this leakage current during write access decreased.Because the dual gate MOS requires less operating voltage.Hence,8-bit,32-bit & 64-bit SRAM cells are designed & their write power is analyzed with respect to single gate.*

Keywords- CMOS, Dual-Gate, Leakage Power, MOS, SRAM.

I. Introduction

The future Moore's law stated that cost per function of the system can be reduced by integration & technology scaling. He verified that the cost per component is nearly inversely proportional to the number of components. But as the number of integrated components is growing in turn the cost per component is raising.These trends directs to a minimum cost in the growth of technology.

1.1 Memory Contribution With Respect To Chips: In digital systems, semiconductor memory arrays are capable of storing large quantities of data.

The amount of memory required in a particular system depends mainly upon the application, but the number of transistors utilized for the data storage is much more.Hence, large area utilization.The increasing demand of large data storage capacity has driven memory development towards more compact design rules.so that higher storage can be done.Thus,the max. Data storage capacity of single-chip semiconductor memory arrays doubles every two years.The area efficiency of the memory array i.e,the number of stored data bits per unit area is the key criteria to determine the storage capacity due to this the cost per bit increases.The another issue is the memory access time required to store & retrieve the particular data bit in the memory array.The access time determines the memory speed.Finally,the static and dynamic power consumption of the memory array is the another factor to be considered in the design because of the increasing demand of low power applications.

1.2 MOS Leakage Power:

MOS suffers from the problem of leakage. There are three major components due to which leakage results in the MOS.The first one is the tunnelling junction leakage current which is due to the dissemination of minority carriers near the edge of the space charge region and also due to the election-hole pair generation in the space charge region in the reversed biased junction. The second suthreshold leakage current results when gate-source voltage is less than the threshold voltage then current drops off exponentially rather than becoming zero. The last is the tunnelling gate leakage current, as the thickness of the gate oxide reduces only to few atomic layers, electrons tunnel through the gate causing some gate current.

1.3 MOS Benefits:

MOS offers various advantages like reduction in device area.The miller capacitance and output conductance are further reduced, making the dual gate MOSFET a useful device for analog integrated circuits.The reduced

feedback and the resulting increase in power gain and stability, in conjunction with the increased functional capabilities stemming from the presence of two independent control gates.The break down voltage can be made very high with proper design.The short channel effects are considerably diminished.

II. Related Work

Many researchers have been working on dual gate SRAM designing and to reduce the read and write delays, some of related research is given below:Behnam *et.al*.(2008)[4]:This paper gives the method to reduce the read and write delays of a memory cell in an SRAM block,the total leakage power dissipation of SRAMs depends upon the physical distance between the different blocks.The method is to organize six-transistor sram cells for different threshold voltage and oxide thickness.Radu M.Barsan *et.al*[19]:In this paper,the operation and physical characteristics of Dual Gate MOSFET are investigated.The static characteristics are analyzed in detail,special emphasis being directed toward the properties of the drain conductance and transconductances in the various operational modes.Besides,this various advantages of dual gate such as increased gain,stability & reduction in short channel effects etc,are also described.B.E Roberds,*et.al*(1998): In this paper[7],a method for fabricating a dual-gate SOI MOSFET is proposed,which involves using ion cut techniques to bare the MOS for buried gate transistor underside processing,the use of a transparent quartz 'handle' wafer onto which the delaminated structure is adhered,the use of the bottom gate as a hardmask for near-field lithography of the top gate,and using through-wafer illumination by g-line light to expose the poly resist.Kavita *et.al*(2008):This paper[23] presents that CMOS SRAM cell is very less power consuming & have less read & write time.Higher cell ratios can decrease the read & write time and improve stability.PMOS transistor with less width reduces the power consumption.This paper implements 6T SRAM cell with reduced read & write time,area & power consumption.It has been noticed that increased memory capacity increase the bit-line parasitic capacitance which in turn slows down voltage sensing and make bit-line voltage swings energy expensive. This result in slower & more energy consuming memories.Koray Karahaliloglu.*et.al* (2001): An analytical current model for the dual-gate MOSFET structures is presented. [11]The standard method for MOSFET modeling is investigated for dual and multi-gate MOSFETs.For the difficulties arising in such methods,an energy-based approximation is introduced to get a quasi-fermi potential solution that will be valid along the channel.An explicit current expression for the dual gate MOSFET is obtained by making use of this solution.

III. Dual Gate MOSFET Designing

It is a special MOSFET with two gates controlling the channel instead of one gate as in the case of traditional bulk MOSFET. The gates surrounding the conducting channel ensures that a better control over the channel can be applied, which reduces the leakage currents, the drain induced barrier lowering and other short channel effects.Since there no schematic models of DGMOSFET available, it has been designed using the equivalent approach in which we have considered two serial connected transistors equivalent to a single DGMOSFET [18].

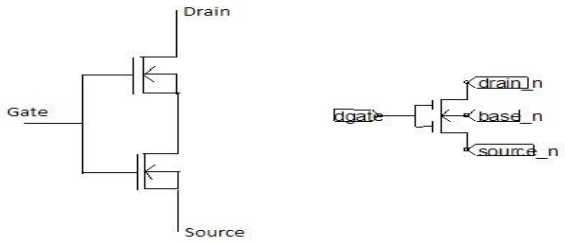


Fig. No.1: Design Equivalent of DGMOSFET.

IV. Inverter

The Dual Gate CMOS Inverter Is Operated on the 5v supply and input is given in the pulse form.It is implemented in TANNER EDA tool as shown below:

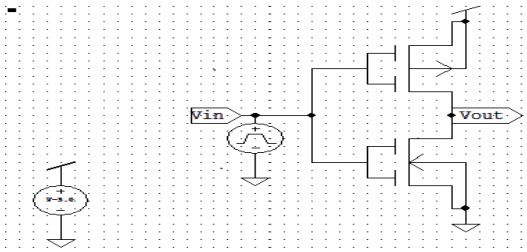


Fig. No.2: Schematic view of inverter.

V. 1-Bit Dual Gate MOSFET SRAM

Fig. 3 shows the conventional 6T SRAM cell. It consists of 2 PMOS and 4 NMOS transistors. The structure is like two cross coupled inverters with two NMOS as word select.CELL OPERATION: We can carry out both write or read operations on the cell. For write operation two signals will be produce from the input data one is 'bl' and another is 'blb'. Where bl = data and blb = complement of data. Then word line (wl) goes high which enables the access transistors and the data will be written in the cell. For read operation both 'bl' and 'blb' lines are pre-charge to voltage Vpre and then 'wl' goes high, since SRAM is already either in state '0' or in '1', then according to the state only one line discharges to Gnd and a voltage difference is establishes between 'bl' and 'blb' lines. This difference will be sensed by sense amplifier and finally stored bit will be available at the output of sense amplifier. From the operation it is clear that the cell dissipate power in two cases, one is during reading and writing the bit, due to switching activity of transistors, and another is when the cell is in idle state, because one transistor from both the inverter is in 'on' state continuously which dissipate power due to leakage current. In addition to this the peripheral circuits such as row decoder, column decoder and sense amplifier also dissipates a lot of power.

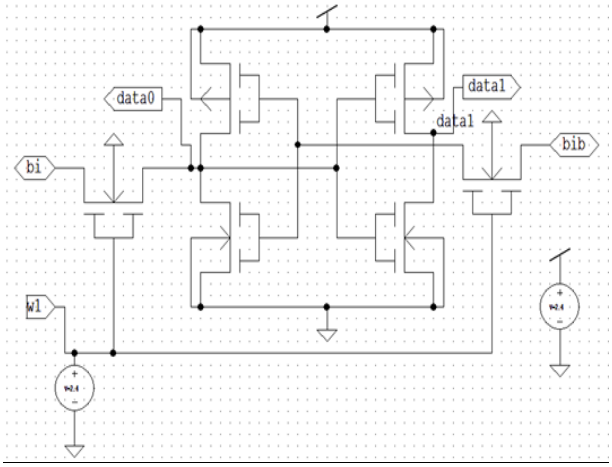


Fig.No.3: Schematic view of 1bit SRAM cell.

VI. 8-Bit (8×1) Dual Gate MOSFET SRAM

Figure.4 shows the schematic of 8-bit (8 × 1) SRAM by using conventional 6T SRAM cell and interfaced with 3 × 8 decoder for row selection from address lines. Nodes 'data0', 'data1', 'data2', 'data3', 'data4', 'data5', 'data6' and 'data7' shown are inside the cells and by plotting the graph for voltage versus time of each nodes we can verify that whether the desired data given at signal 'data' has been correctly written inside the cells or not. The circuit consists of 106 transistors out of which 33 are PMOS and 73 are NMOS transistors.

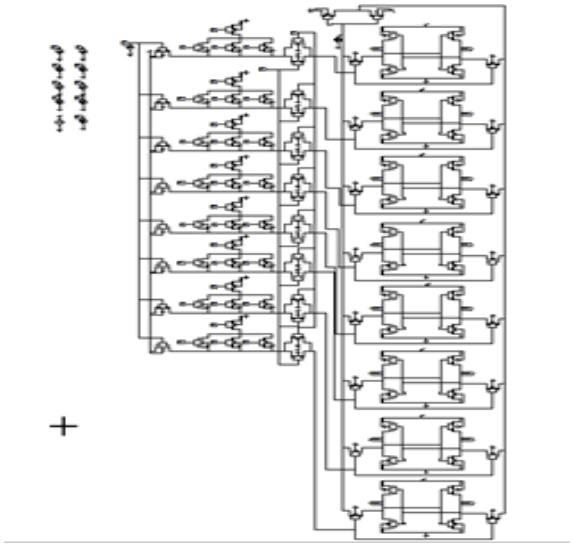


Fig.No.4: Schematic view of 8-bit SRAM cell.

VI. Comparison

Table. I shows the comparison of power between single gate and dual-gate SRAM for different techniques. It includes the results of work presented in this paper. The conventional 6T SRAM consumes $6.75*10^{-004}$ watt ,$6.84*10^{-004}$ watt ,$9.79*10^{-004}$ watt and $1.16*10^{-003}$watt at 180µm, 200µm,125µm and 0.13µm respectively which is reduced when Dual-Gate MOS is used. The Dual-Gate MOS 6T SRAM consumes $1.18*10^{-005}$,$5.66*10^{-004}$,$8.25*10^{-006}$ and $4.23*10^{-005}$ at 180µm, 200µm,125µm and 0.13µm respectively.

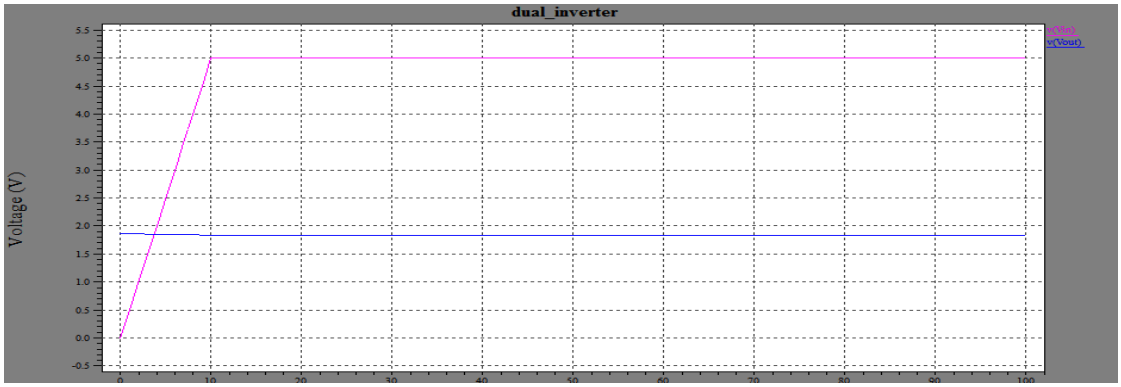
VII. Conclusion

In this paper, Dual gate SRAM design techniques are discussed. Dual Gate SRAM reduces the write power consumption due to less operating voltage.The gates surrounding the conducting channel ensures that a better control over the channel can be applied, which reduces the leakage currents, the drain induced barrier lowering and other short channel effects.

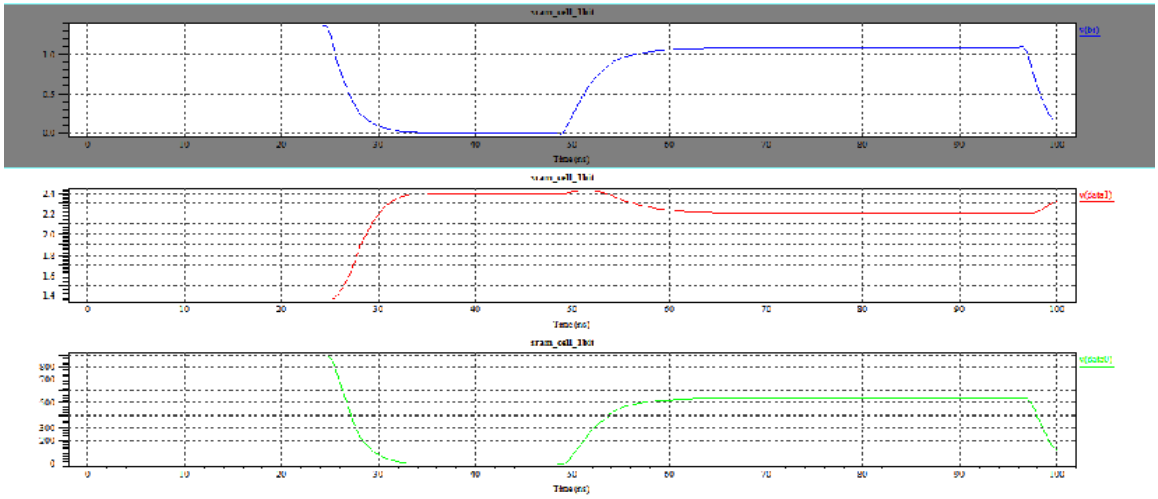
Table I. Comparison of power for different technologies for 6T SINGLE GATE SRAM & 6T DUAL GATE SRAM

TECHNOL-OGY	6T SINGLE GATE SRAM			6T DUAL GATE SRAM		
	Average Power(in watts)	Maximum Power(in watts)	Minimum Power(in watts)	Average Power(in watts)	Maximum Power(in watts)	Minimum Power(in watts)
180µm	$6.75*10^{-004}$	$1.638*10^{-002}$	$2.38*10^{-010}$	$1.18*10^{-005}$	$1.04*10^{-003}$	$8.18*10^{-011}$
200µm	$6.84*10^{-004}$	$3.79*10^{-003}$	$1.37*10^{-006}$	$5.66*10^{-004}$	$5.22*10^{-003}$	$2.41*10^{-006}$
125µm	$9.79*10^{-004}$	$6.37*10^{-003}$	$1.95*10^{-007}$	$8.25*10^{-006}$	$2.03*10^{-002}$	$3.09*10^{-007}$
0.13µm	$1.16*10^{-003}$	$3.65*10^{-003}$	$2.96*10^{-005}$	$4.23*10^{-005}$	$3.51*10^{-004}$	$4.30*10^{-007}$

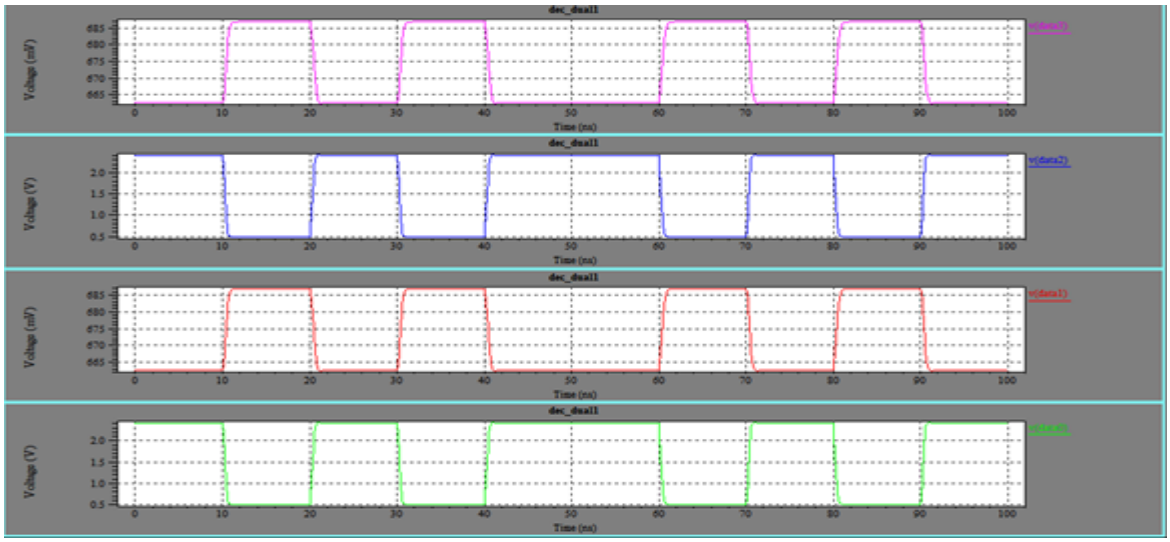
Output Simulation Waveform of Dual Gate Inverter



Output Simulation Waveform of Dual Gate 6T SRAM



Output Simulation Waveform of 8-Bit (8×1) Dual Gate SRAM



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