RESEARCH INVENTY: International Journal of Engineering and Science
ISSN: 2278-4721, Vol. 1, Issue 9 (November 2012), PP 46-52
www.researchinventy.com

Digitally Controlled Current-Mode Dc–Dc Converter Ic

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Abstract: *The main focus of this paper is the implementation of mixed-signal peak current mode control in low-power dc–dc converters for portable applications. A DAC is used to link the digital voltage loop compensator to the analog peak current mode loop. Conventional DAC architectures, such as flash or are not suitable due to excessive power consumption and limited bandwidth of the reconstruction filter, respectively. The charge-pump based DAC (CP-DAC) used in this work has relatively poor linearity compared to more expensive DAC topologies; however, this can be tolerated since the linearity has a minor effect on the converter dynamics as long as the limit-cycle conditions are met. The CP-DAC has a guaranteed monotonic behavior from the digital current command to the peak inductor current, which is essential for maintaining stability. A buck converter IC, which was fabricated in a 0.18 m CMOS process with 5 V compatible transistors, achieves response time of 4 s at for a 200 mA load-step. The active area of the controller is only 0.077 mm and the total controller current-draw, which is heavily dominated by the on-chip senseFET current-sensor, is below 250 A for a load current of 50mA.*

Index Terms: *CPM, current-mode, dc–dc converter, digital con- trol, integrated circuits, power management, SMPS, voltage regu- lators.*

1. Introduction

High-Frequency dc–dc converters are increasingly being integrated into system-on-chip (SoCs) designs, in order to provide one or more tightly regulated supply voltages for various mixed-signal blocks. In most low-power applications, the power conversion efficiency of the converters must be maximized over the full range of operating current. At the same time, the PCB footprint of the filter components should be minimized by operating at the highest possible switching frequency, which makes low-power design very challenging. In sub-1 W applications, the controller power-consumption must be minimized to avoid degrading the overall converter efficiency. A typical experimental efficiency versus load-current curve is shown in Fig. 1. The maximum current draw of the controller operating in PWM mode is also shown for an efficiency degradation ranging from 0.2% to 2%, which is considered acceptable. Below I_{out} mA, the total controller cur- rent-consumption is limited to 250 A for an efficiency degradation of 0.2%, which is very challenging for high-performance, high-frequency controllers.

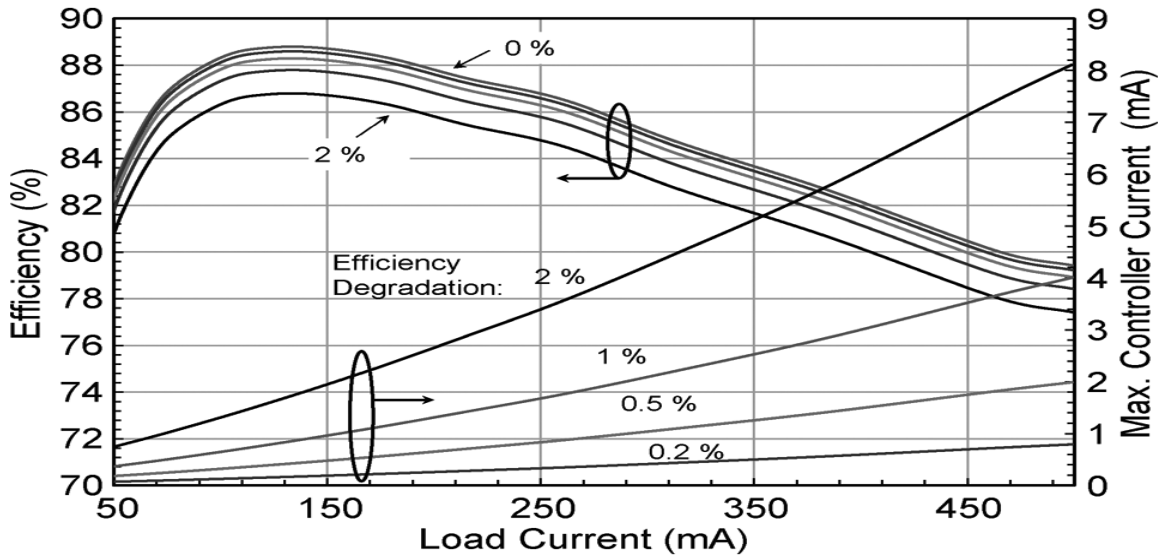

Fig. 1. Efficiency degradation due to controller power consumption.

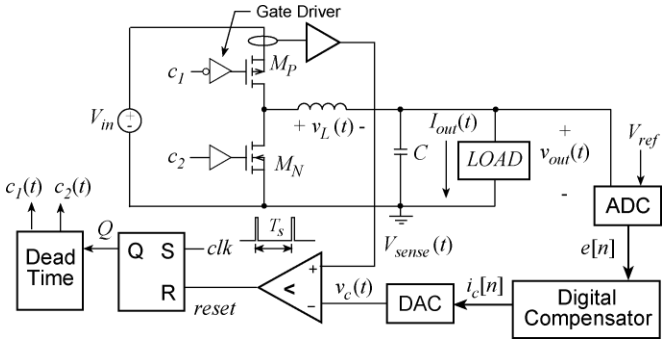

Fig. 2. Synchronous buck converter with mixed-signal current mode control.

Below several hundred MHz, full monolithic integration in CMOS processes is not feasible today, due to size and cost con- straints for the passive components [1]. Instead, the system-in- package (SiP) solution is gaining momentum for high-efficiency onversion in the several-to-ten's of MHz range. SiP consists of packaging the die and passives together to reduce the footprint and parasitics [2]. Several dc–dc converters having in-package inductors that use proprietary packaging/integration techniques have been introduced [2]–[4]. Including the inductor in the same package as the die allows further optimization of the efficiency compared to traditional designs, where the inductor characteristics are unknown to the IC manufacturer. This work is targeted to SiP applications in the 2–10 MHz range. Peak current-mode control (CPM) provides inherent cycle-by-cycle current-limiting in the power transistors and simplified loop dynamics, which allows simple and robust compensation of the control-loop [5] as shown basic architecture was first reported in [16]. In addition to providing numerous additional implementation details and new measurement results, this paper examines the effect of charge/discharge current mismatch inside the charge- pump on the converter's closed-loop operation and reaches new conclusions about the application range of this topology. This paper also investigates the effect of current source mismatch in the DAC architecture. This paper is organized as follows. The limit-cycle phenomenon for mixed-signal CPM is analyzed in Section II, leading to minimum resolution requirements for the DAC. The pro- posed low-power DAC architecture for linking the voltage and current loops is presented in Section III. The high-bandwidth analog current sensing scheme is presented in Section V and experimental results for the fabricated prototype are reported in Section VII.

2. Limit-Cycle Oscillations In Current-Mode Control

Unless otherwise stated, it is assumed that the converter runs in CPM without slope-compensation, which implies that the steady-state duty-cycle is limited to in order to avoid inherent instability in the current loop [5]. Instability in the un- compensated current loop has been shown to appear slightly below[17].Thetwoquantizers (the DAC and the ADC) in the feedback loop make hybrid CPM prone to limit-cycle oscillations, a phe- nomenon which is well understood in digital voltage-mode controllers [18], [19]. In this section, the analysis method presented in [18] is extended for the hybrid CPM. The DC output voltage change caused by changing the DAC input by one LSB, , is given bydomain, while the current-regulation loop has a traditional analog implementation. Using this architecture, a DAC is required at the interface of the two loops, in order to generate an analog current command. Mixed-signal CPM benefits from the simplicity of the analog current loop and the flexibility of the digitally compensated voltage loop. With this approach, a reconfigurable digital compensator can be used without the need for sampling the inductor current. The high-frequency digital pulse-width modulator (DPWM) required for fully digital CPM schemes [12]–[14] is also eliminated, resulting in a practical, low-cost implementation.The design of a low-power DAC specialized for mixed-signal CPM is the main focus of this work. A flash architecture is not appropriate due to high power consumption, which limits the light-load efficiency of the buck converter. In [11], a one-bit DAC was used to meet the tight resolution requirements of mixed-signal CPM; however, the low-pass reconstruction filter in the DAC introduces an undesirable pole in the system transfer function. This pole limits the control bandwidth and overall regulation performance. An adaptive control scheme was developed to address this issue [11], where the DAC over-sampling rate and filter corner frequency of the DAC are varied in real-time to achieve both low steady-state power consumption and fast transient response. In this work, the aim is to eliminate the main shortcomings of the previous

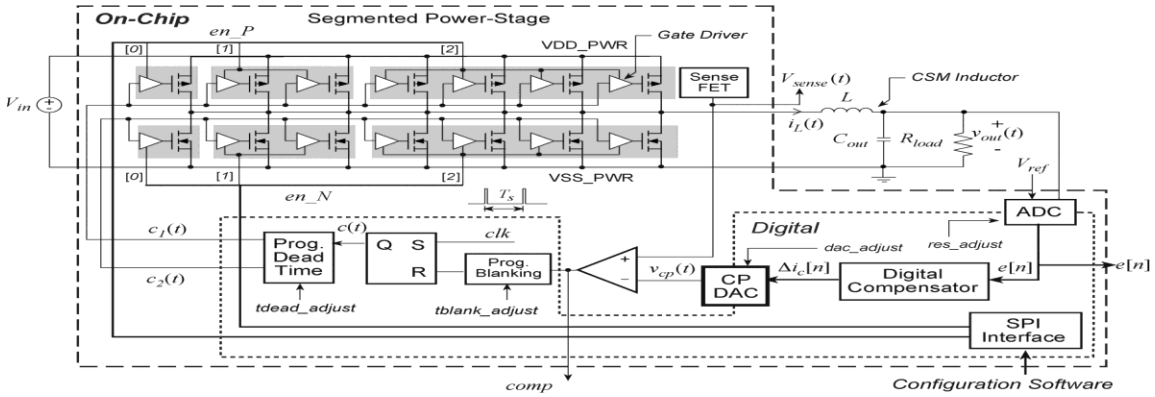

Fig. 3. Simplified architecture of the integrated dc–dc converter with a hybrid CPM control scheme and the novel DAC.

DAC approach, namely f_s, the bandwidth restriction imposed by the DAC's low-pass filter, while at the same time generating a high resolution voltage reference for the current-loop. The simple low-power DAC architecture is applied to the hybrid scheme for a synchronous buck converter IC, as shown in Fig. 3. The IC includes the control circuits, as well as a segmented power-stage [15] for improving light-load efficiency. Unlike other topologies topologies, the proposed DAC does not require extensive digital signal processing (noise shaping) or high-frequency clocks beyond the switching frequency. The CP-DAC basic architecture was first reported in [16]. In addition to providing numerous additional implementation details and new measurement results, this paper examines the effect of charge/discharge current mismatch inside the charge- pump on the converter's closed-loop operation and reaches new conclusions about the application range of this topology. This paper also investigates the effect of current source mismatch in the DAC architecture.This paper is organized as follows. The limit-cycle phenom- enon for mixed-signal CPM is analyzed in Section II, leading to minimum resolution requirements for the DAC. The pro- posed low-power DAC architecture for linking the voltage and current loops is presented in Section III. The high-bandwidth analog current sensing scheme is presented in Section V and experimental results

TABLE I SYSTEM SPECIFICATIONS

Specification	Value	Units
Input Voltage, V_{in}	2.7-4.2	V
CMOS Process (HV)	0.18	μm
Output Voltage, V_{out}	1	V
Rated Load, I_{load}	0.5	A
Filter, L	1	μH
Filter, C_{out}	4.7	μF
Switching Frequency, f_s	3	MHz
ADC Error Bin (zero error), ΔV_{adc}	13	mV
ADC Error Bin (other bins), ΔV_{adc}	6	mV
ADC Conversion time $t_{conv,adc}$	162	ns
DAC resolution, ΔV_{dac}	2.2	mV
Closed-loop Load Step Response	< 4	μs

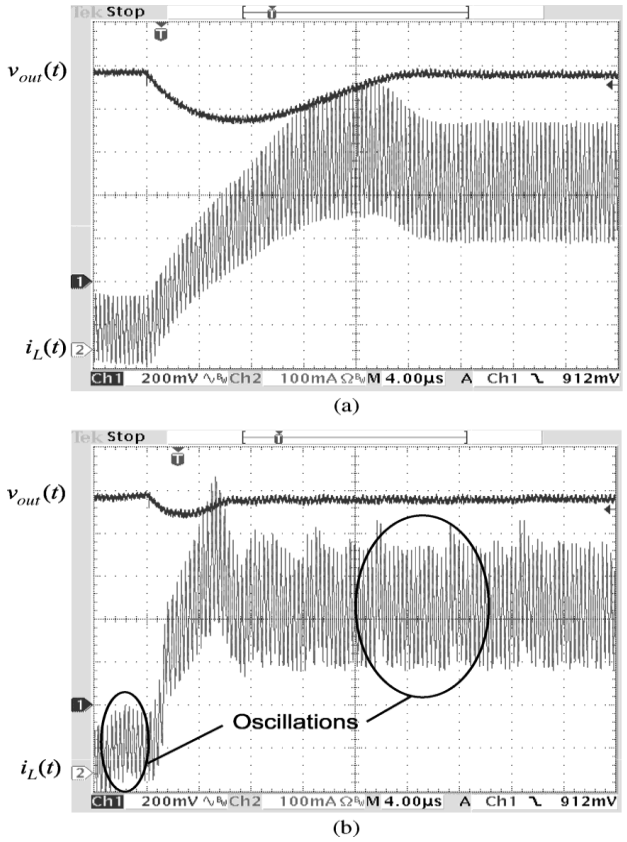

Fig.4. Load-step response showing the effect of decreasing by 2.5 from (a) to (b).

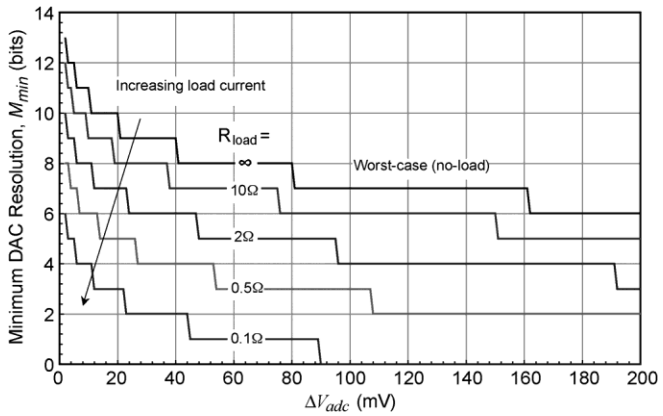

Fig. 5. Minimum DAC resolution for different values of .

The minimum resolution is highly load dependent. The resolution requirements in DCM mode are analyzed in [20]. The presence of limit-cycle oscillations in the inductor current is con- firmed experimentally in the load-step response of Fig. 6. For a fixed DAC resolution, reducing the sensing gain K_s. The oscillations in Fig. 4(b) disappear when the voltage loop is opened, proving that the oscillations are due to the outer regulation loop. The result is shown in Fig. 5, for the parameters of Table I. The high control-to-output gain in CPM results in a higher resolution requirement for the DAC, compared to the DPWM in voltage-mode control. It can be seen that unlike voltage-mode control in continuous-conduction mode (CCM), the minimum resolution is highly load dependent. The resolution requirements in DCM mode are analyzed in [20]. The presence of limit-cycle oscillations in the inductor current is con- firmed experimentally in the load-step response of Fig. 4. The output voltage versus current command, obtained from solving (6), is shown in Fig. 6(a) for different values of $R_{\rm load}$ and for the parameters given in Table I. The current-loop gain from (7) is plotted in Fig. 4(b). In both cases, the duty-cycle limit of is shown by the dashed line, beyond which the current loop is inherently unstable [5].

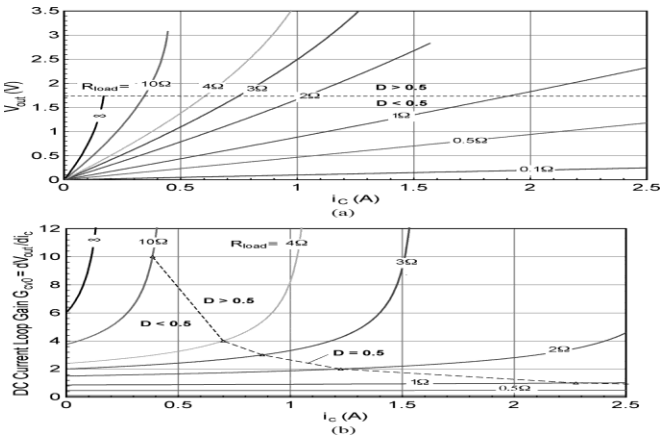

Fig. 6. (a) Output voltage versus current-command and (b) small-signal gain for different values

3. CLOSED-LOOP RESPONSE

An accurate system model was generated in Matlab/ Simulink, based on the extracted parameters of the power-stage and the mixed-signal blocks, as well as the finite precision of the digital registers in the digital compensator. The simulated step-response for the closed-loop system is shown in Fig. 14(a) and (b) for 50–250 mA and 50–500 mA load steps, respectively. The output voltage is regulated back into the zero-error bin $(e[n] \quad 0)$ within about 5 s for a load-step of 50–250 mA. The differential current-command waveform shows that the CP-DAC immediately adjusts the peak inductor current following the load-step. The system parameters are summarized in Table I. As mentioned in Section III, the mismatch in the bi- nary-weighted sources in the programmable current sink can lead to a no monotonic characteristic from despite the fact that $v_{\rm cp}(t)$ is monotonic with respect to the target $i_c[n]$. This effect was investigated by simulating the converter in closed-loop with different combinations of mismatch in the binary weighted current sinks of Fig. 6, ranging from 0 to 20% of. The ideal ratios were varied from. The overlapped CP-DAC input/output characteristics are shown in Fig. 7(a). The figure also includes the characteristic for an ideal DAC with uniform quantization. The resulting 29 closed-loop responses are overlapped in Fig. 7(b). The simulation confirms that the response is stable in all cases, with only minor differences in the settling time and voltage fluctuation.

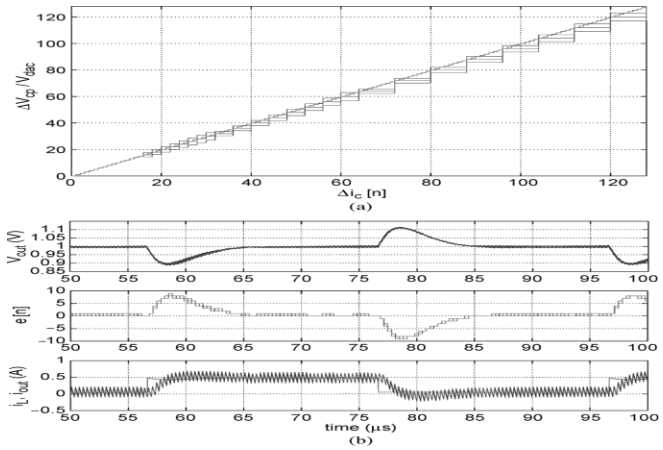

Fig 7 (a) Overlapped CP-DAC input/output characteristic for different combinations of the current sink ratios in the CP-DAC. (b) Overlapped closed-loop 50–500 mA load-step responses for the 28 combinations of CP-DAC characteristics, showing the minor effect of the CP-DAC nonlinearity.

4. EXPERIMENTAL RESULTS

The converter shown in Fig. 8 includes a segmented power- stage similar to [29] for improved light-load efficiency. It was fabricated in a 0.18 m CMOS process with 5 V transistors, which are sufficient to accommodate the single-cell lithium-ion battery voltage range of 2.7 V to 4.2 V. The chip micrograph is shown in Fig. 17. The die measures10mm, while the total active area for the controller (excluding the power-stage) is only 0.077 $\rm mm^2$. The total controller current-draw, which is dominated by the on-chip senseFET current-sensor, is below 250 A at 1 0 mA. The current-draw and active area of each block are given in Table II.

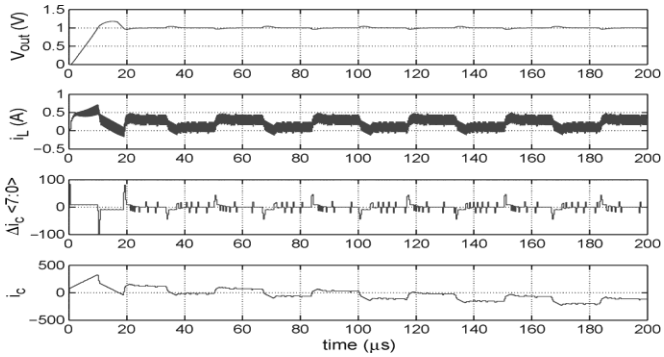

Fig. 8. Simulated closed-loop response with a 15% mismatch between the charge and discharge currents in the CP DAC.

Table Ii
Summary Of Area And Power Consumption For The Controller Portion Of The Cpm Ic

IC Block	Area (mm^2)	Current-Draw (μA)	Current-Draw (μA/MHz)	Condition V_{in} = 3.7V V_{out} = 1V f_s= 3MHz
Charge Pump DAC	0.0135	2.96	0.98	Steady-state
Delay-Line ADC	0.0295	25.9	8.65	Steady-state
SenseFET Core	0.0029	123	41.2	I_{out} = 50 mA
		169	56.6	I_{out} = 250 mA
		227	75.8	I_{out} = 500 mA
CPM Comparator	0.0011	59	19.7	
Dead-Time	0.0078	5.46	1.82	
Bias+Reference	0.0018	23.2	7.73	
Digital Core	0.0205	10	3.3	Steady-state
Total	0.0770	249.5	83.2	I_{out} = 50 mA
		295.5	98.8	I_{out} = 250 mA
		353.5	117.8	I_{out} = 500 mA

5. CONCLUSION

A low-power solution has been proposed for implementing mixed-signal peak current-mode control in dc–dc converters for portable applications. The charge-pump DAC has relatively poor linearity compared to more expensive DAC topologies; however, this can be tolerated since the system runs in closed-loop. The CP-DAC has a guaranteed monotonic behavior from the digital current command $i_c[n]$to the peak inductor current which is essential for maintaining stability. It was shown that mismatches in the charge and discharge currents in the charge-pump make it impossible to internal store $i_c[n]$in the digital domain without using some form of calibration. This is not a major limitation since many linear and nonlinear digital compensators can be implemented simply by calculating $\Delta i_c[n]$ each cycle. A major advantage of the CP-DAC over flash and architectures is the fact that it consumes nearly zero current when the dc–dc converter is in steady-state. The power consumption of the CP-DAC scales with the frequency of the load transients. The prototype IC has a fast transient response which can be further improved by using a more sophisticated compensator. The operating frequency was primarily limited by the bandwidth of the current sensor, since the power-stage can easily operate beyond 10 MHz. The output voltage range can easily be extended by implementing traditional analog slope compensation.

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