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Design of 16-QAM Transmitter and Receiver: Review of Methods of Implementation in FPGA

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Abstract *- FPGAs provide magnificent speed of operation of sophisticated algorithms at sample rates of hundreds of MHz. This kind of processing power makes it possible to use FPGAs for implementing not only conventional baseband functionality but also high-speed signal processing. This paper is a demonstration of complete system generator based design of 16-QAM transmitter which can be easily implemented in FPGA as compared to the existing models. This modulation scheme is used in many communication standards such as IEEE802.11a, IEEE 802.16d and DVB-S2. The existing architectures of both QAM transmitter and receiver consider the real time design issues like symbol mapping, source encoding, IF up-conversion, channel coding, IF down-conversion, Receiver decoding, carrier & phase recovery, timing synchronization and most importantly equalization. But unfortunately none of them suggest a complete architecture taking all the design issues into account. However this paper summarizes the advantages and disadvantages of all the architectures suggested so far and aims to have a complete system generator based transmitter model which can be practically implemented in FPGA.*

Keywords *- 16-QAM, Symbol Mapping, Interpolation, up conversion, down conversion, FPGA design*

1. INTRODUCTION

The development in the modulation techniques had been witnessed since last two decades which demands reliable transmission of information with higher data rate. Due to more resistible to noise digital modulation techniques have created an interest. At present FPGAs and ASICs are playing a vital role in designing, simulating, testing and implementing the new communication techniques. Moreover system level design and implementation is possible due to tools like system generator which facilitates testing algorithms, modifying designs as per the requirement very easily. Modulation scheme such as QAM is one of the widely used modulation techniques in cellular communication because of its high efficiency in power and bandwidth16-QAM (Quadrature Amplitude Modulation) is a kind of digital modulation scheme which transmits four bits per symbol on two orthogonal carriers; one in phase and the other one is in quadrature phase. Hence the data rate is increased by a factor of four. It is quite preferable as there is a balance between obtaining the higher data rates and maintaining an acceptable bit error rate keeping the energy of the constellation constant.The remaining of the paper is presented as follows: section 2 demonstrates the review of some basics of QAM and simulation of a simulink based model. In section 3 the different methods till now adopted to implement QAM in FPGA and corresponding merits and demerits are described. Section 4 proposes the complete system generator based transmitter model and simulation results. Section 5 points out the FPGA resources used and finally conclusion is discussed.

2. QAM BASICS & SIMULINK BASED MODEL

In Quadrature Amplitude Modulation technique data is sent by varying both amplitude and phase of the carrier signal. Generally two carrier waves are taken which are orthogonal to each other. Four bits are grouped by taking two bits from each carrier to form a symbol. The number of possible symbols is 2^4=16 and one of these 16 possible signals is transmitted at each symbol period [1]. The general form of a 16 QAM signal can be defined as:

$$s_i(t) = \sqrt{\frac{2E\min}{Ts}} a_i \cos 2\pi f_o(t) + \sqrt{\frac{2E\min}{Ts}} b_i \sin 2\pi f_o(t)$$
$$0 \le t \le T_s, i = 1,2,3,..,16 \quad \text{.....(1)}$$

Where $E_{\min}$ is the energy of the signal with the lowest amplitude, a_i and b_i are a pair of independent integers chosen according to the location of the particular signal point; f_0 is the carrier frequency; Ts is the symbol period.

The coordinates of the i_{th} message points are $a_i\sqrt{E_{\min}}$ and $b_i\sqrt{E_{\min}}$ where (a_i, b_i) is an element of the 4 by 4 matrix as shown below.

$$(a_i, b_i) = \begin{bmatrix} (-3,3)(-1,3)(1,3)(3,3) \\ (-3,1)(-1,1)(1,1)(3,1) \\ (-3,-1)(-1,-1)(1,-1)(3,-1) \\ (-3,-3)(-1,-3)(1,-3)(3,-3) \end{bmatrix}$$

In digital modulation techniques, the constellation diagram is used to represent the complex amplitude of each possible symbol state graphically. The constellation diagram of 16-QAM is shown in Fig. 2.Xiaolong Li (2008) proposed the simulink based model of 16-QAM. The authors have implemented the same in simulink environment and simulated. The architecture and the results are shown in Fig. 1 and Fig. 2 respectively. Further [1] describes the variation of error rate with SNR excellently up to simulation level, but doesn't give any idea to implement QAM system in real time hardware like FPGA. The model proposed also takes the basic QAM modulator and demodulator blocks along with channel from simulink library, so doesn't consider any of the critical phenomena like carrier synchronization, equalization etc.

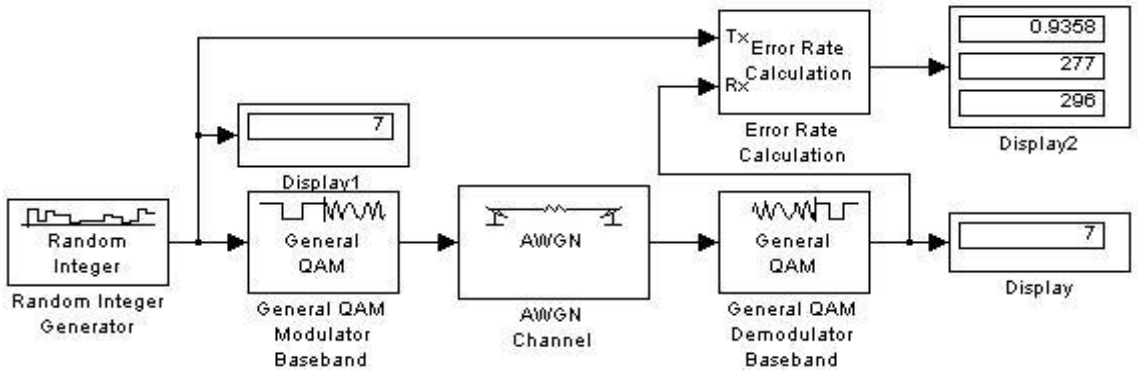

Fig. 1. Simulink based model of 16 QAM

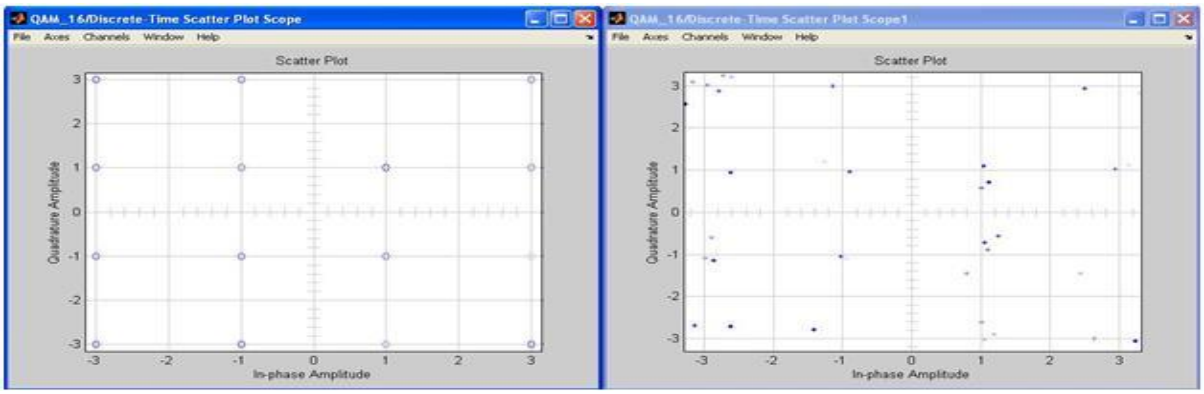

Fig. 2. Constellation diagram before and after channel

3. METHODS PROPOSED TILL NOW FOR IMPLEMENTATION IN FPGA

Many methods till now proposed to implement QAM in FPGA by taking the different design issues separately which are mentioned as follows. In one of the researches Chris et al. (2002) focused on carrier synchronization in QAM system [2], [3] based on Digital Phase Locked Loop (DPLL) and designed an all-digital-receiver. The DPLL requires a 2-D slicer, phase detector, loop filter and Direct Digital Synthesizer (DDS). The phase detector is implemented in two ways; one is memory based and another one is based on

Coordinate Rotation Digital Computer (CORDIC) [4]. They had implemented this receiver in FPGA which lacked timing synchronization and equalization. In another paper Chris et al. described about adaptive equalizers which operate to minimize inter symbol interference (ISI), due to channel-induced distortion, of the received signal [5]. The equalizer operates in cascade with a matched filter (MF), synchronous sampler, and decision device (slicer) operating at the symbol rate. The phase error in the received signal can be minimized by an adaptive equalizer. The system generator library provides a complete demo diagram of 16-QAM baseband demodulator [6]. This diagram mainly considers equalization and carrier recovery. Phase error is corrected by fast computing tool CORDIC. LMS algorithm based equalizer is used to reduce ISI and make the constellation correct. However if any delay is introduced in the transmission line this model fails due to lack of timing synchronization. Moreover this model can't be applied to deep fading channels due to lack of IF up and down conversion. The demo model is given in figure 3.Helen et al. in [7] and Stephen et al. (2008) in [8] described about the Digital Up Converter (DUC) and Digital Down Converter (DDC) which are highly essential for RF transmission in wide band as well as narrow band systems. The function of the DUC is to translate one or more channels of data from baseband to a pass band signal comprising modulated carriers. It is done by interpolation to increase the sample rate, filtering to provide spectral shaping and rejection of interpolation images, and mixing to shift the signal spectrum to the desired carrier frequencies.

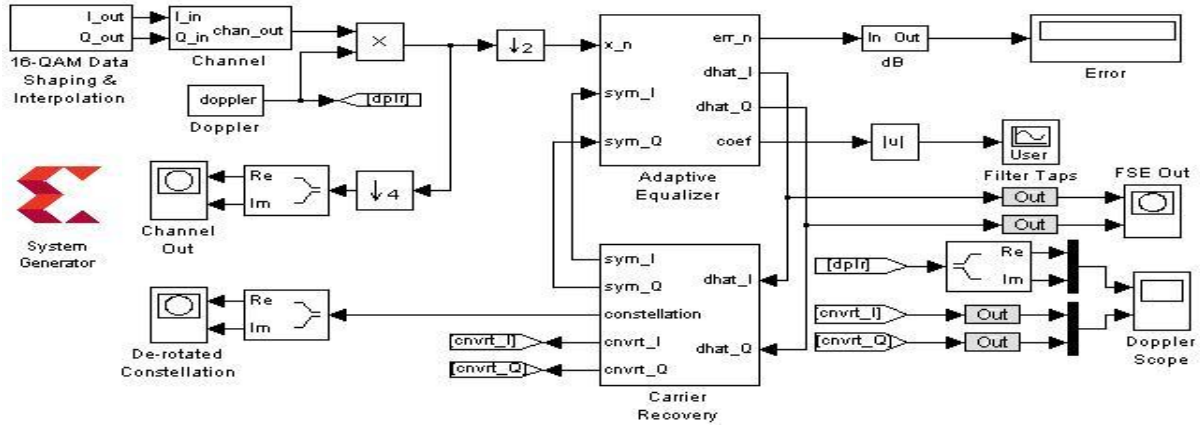

Fig. 3. 16-QAM demodulator demo from Xilinx

The function of DDC is to translate a passband signal comprising of one or more high frequency carriers to one or more baseband channels for demodulation and interpretation. These concepts are highly applied during the design of transmitter and receivers separately which are connected by a deep fading channel. Narinder Lall (2006) has modeled QAM with coding and implemented in FPGA [9]. He has used block codes such as Reed-Solomon (RS) encoder and convolution encoder for encoding purpose; whereas viterbi decoder and RS decoder for decoding purpose. But it lacks IF up and down conversion. Majid et al. (2009) had proposed a system generator based model for 16-QAM transceiver [10]. This model certainly considers all the previously mentioned design issues and beautifully produces the results by implementing it in FPGA. It implements a transceiver by taking the AWGN channel block present in simulink. The IF-to-RF conversion and RF-to-IF conversion is done purely in analog domain. However this model doesn't include any coding techniques. Finally Xuan-Thang et al (2010) have studied QAM from all the design issues point of view and presented an excellent model [11]. They implemented the transmitter and receiver in two separate extreme DSP FPGA kits which supports on board ADC and DAC. The key point of this model is they have implemented the timing synchronization, IF up and down conversion and all are in digital domain. But this model also doesn't take care of coding techniques and it implements only a standard sequence as the pilot sequence.

4. PROPOSED SYSTEM GENERATOR BASED TRANSMITTER MODEL

The transmitter can be designed easily from the principle block diagram of 16-QAM which consists of two main parts: data block and IF block [1]. First two independent signals are generated which carries the bits to be transmitted. Then one channel X_i (the one "in phase") is multiplied by a cosine, while the other channel X_Q (in "quadrature") is multiplied by a sine. This way there is a phase difference of 90° between them. They are simply added one to the other and sent through the channel.
The sent signal can be expressed in the form:

$$s(t) = \sum_{n=-\infty}^{\infty} \left[v_c[n] h_t(t - nT_s) \cos(2\pi f_0 t) - v_s[n] h_t(t - nT_s) \sin(2\pi f_0 t) \right] \quad \text{..... (2)}$$

Where $v_c[n]$ and $v_s[n]$ are the voltages applied in response to the n^{th} symbol to the cosine and sine waves respectively. The proposed model has been shown in fig. 4. Two random integer generators are used for data source. Each generates four values at each clock pulse which are carried by two carrier signals I and Q. The symbol mapping block converts these four values to (-3, -1, 1, 3) which can be traced in standard constellation. The symbol mapping block consists of adder and multiplier blocks. Then the signal is up converted and filtered. A 32-tap 4 interpolation MAC FIR filter is used for this purpose. After pulse shaping and up-converting the baseband signal, the signal spectrum is shifted from centered at 0 Hz to an intermediate frequency in the range of [-Fs, Fs] where Fs is the sampling frequency. This process requires a counter, two ROMs and a mixer. The counter counts from 0 to 63. The ROMs find out the corresponding sin and cosine values and store them. In this case the mixer is basically a complex number multiplier which multiplies the up-sampled signals (interpolation filter output) with the complex exponential generated from the ROM. Fig. 5 shows the transmitter constellation and fig.6 demonstrates the interpolated output.

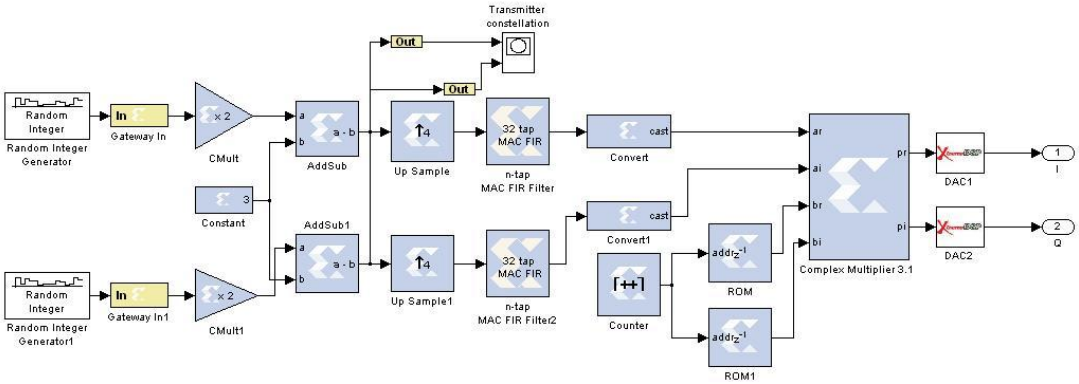

Fig. 4. System generator based 16-QAM transmitted model

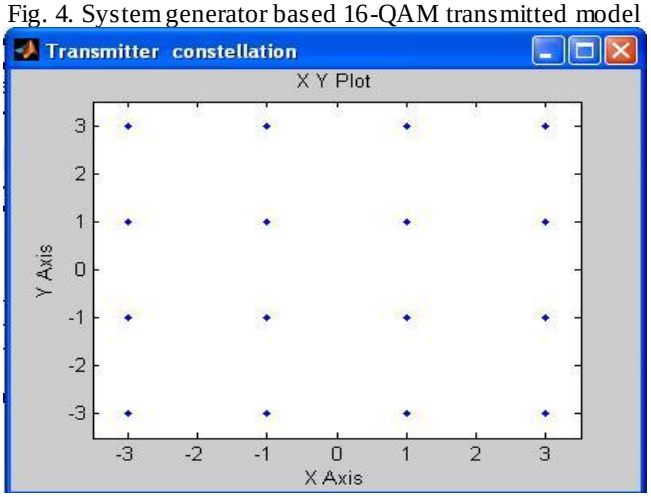

Fig. 5. Transmitted Constellation

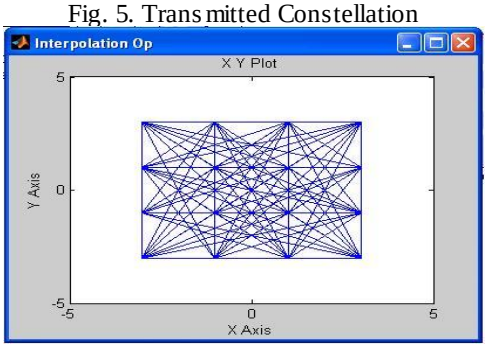

Fig. 6. Interpolation Output

5. RESULTS AND CONCLUSION

The proposed model is simulated in simulink. Then the corresponding VHDL code is generated using system generator tool. The bit file is generated after successfully synthesizing the model and implemented in DIGILENT ATLYS Spartan6 FPGA kit. Fig.7 shows the resources used and available in the FPGA.

Table 1: Resources used

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	394	54576	0%
Number of Slice LUTs	295	27288	1%
Number of fully used LUT-FF pairs	218	471	46%
Number of bonded IOBs	71	218	32%
Number of BUFG/BUFGCTRLs	1	16	6%

Design issues like suitable coding techniques can be applied to this model. A partial system generator based receiver model is present in Xilinx demo models. That model in combination with the proposed model can be demonstrated as a complete model. The review of different research works on 16-QAM shows that models proposed so far are taking only some of the design issues into consideration each. Still research needed to propose a complete 16-QAM model with the aim to contribute in the field of digital modulation.

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