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Design of Compliant Passive Digital Block of Read-Only RFID Tag

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Abstract— *In recent years, low cost RFID is increasingly becoming popular. Tags of such an RFID system consists of less complex architecture, thereby minimizing the power consumption and cost will be less.The work incorporates ISO 14443 regulations for designing the digital block of tag. It utilizes 13.56 MHz carrier frequency which is available worldwide as an ISM (Industrial-Scientific-Medical) frequency. To reduce complexity, the tag is made passive with the only available power source as inductively coupled electromagnetic field of the reader. For further simplicity, a read-only tag has been designed which just reveals its identity to the reader. The tag architecture is divided into two parts: analog and digital blocks. The components of analog block have been designed to reduce the leakage power. Asynchronous logic has been used in digital block to minimize the clock activity and hence cause a reduction in transient power.We have used Type A specifications of ISO 14443 for digital block of RFID tag. This gives the Interrogation field strength Hmin of the reader as 7.5 A/m. From the values of tag dimensions (85.72mm × 54.03 mm × 0.76mm), carrier frequency (13.56 MHz) and no. of antenna turns (N=4), we get the min. rms value of voltage available to the tag U_2 as 2.581V. A Low dropout regulator supplies the voltages for the digital block. The digital block utilizes an asynchronous counter to derive their timing and processing signals. 128 bit ROM stores an EPC (Electronic Product Code) which is fetched, processed and sent back to the reader via decoder, multiplexer and modulator units. As specified in ISO 14443 Type A, the modulation type is 10% ASK with the data rate as 106 kbps.The entire deign has been simulated with an input power source of 600µW. The digital circuitry is implemented on 1V rail to rail voltage to reduce the power consumption. The digital schematic has been simulated on 0.18µm CMOS technology Level 53 models from TSMC and Mentor Graphics EDA tool suite.*

Keywords— *Asynchronous counter, Decoder, Multiplexer, ROM and Modulator.*

1. INTRODUCTION

The above diagram depicts the arrangements of various digital components in the transponder with the memory. All the timing signals are derived in asynchronous fashion from the asynchronous counters. They have been progressively sized to minimize the delay and rise-fall times. Appropriate delays have been added in their path to make a group of signals reach in the same time to a particular block. A decoder has been used to pre-fetch the ROM data. Decoder is made up of conventional NAND gates with modular design. A separate module has been designed for a particular set of input signals. Then these modules are combined strategically to form the entire decoder. The memory block is made up of a MOS NOR ROM with minimum sized NMOS transistors. It gives us the advantage of simplicity in its design over MOS NAND ROM. Although the area occupied is significant compared MOS NAND ROM but it does not concern the design because the area of the antenna is much larger than the integrated components. To sequence the data available at the bit line of the memory a multiplexer has been used. Its selection lines have been derived from the counters to place the data at its output at a particular rate. Conventional NAND gates multiplexer have been used with appropriately sized transistors so to avoid glitches at the output. The data provided by the multiplexer is now encoded using Manchester Coding as specified in the ISO 14443 Type A regulation. A clock has been derived from the counter for the coding. This clock is then fed to a XOR gate along with the data to get the coded data. An ASK Modulator which essentially is an AND gate is used for the first level of ASK modulation. It provides for 100% modulation index i.e. when the coded data is high, the subcarrier is allowed to pass through the gate else it is blocked. This forms the input to be fed to the second level of ASK Modulator which provides for Load Modulation.

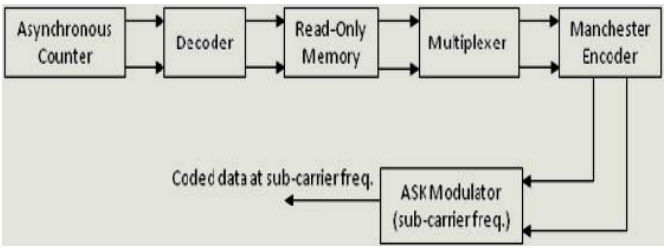

Figure 1 Internal architecture of digital block

Digital Block Design

The digital block contains the modules for data storage, data fetching and data processing. As we have extracted the clock, we have a common reference signal for our design to adjust the data rate as specified in the ISO 14443 specifications and generate other timing signals. Now the choice is ours to use Synchronous or Asynchronous styles of digital designing. Usually synchronous logic has been the choice for many years for digital designers because of its simplicity and reliability for a complicated system. But for a standalone system like ours where power is major issue, asynchronous design seems to be the matter of choice. Also we are aware that the tag is passive and most of the power available to the tag is consumed by Analog part, the Digital has to complete its operation in very less amount of power typically within 20µW. Hence it is very important to keep the no. of operations to minimum for completing the entire operation of it. The asynchronous design plays an important role here because the extracted clock or rather the reference signal derived goes to the input of only one memory device and rest of the memory elements derive their input from the subsequent generated signals and not directly from the clock. Whereas if we use synchronous methodology then the clock must be supplied to each of the memory storage elements thereby increasing the no. of transitions per input cycle of the clock causing an over head to the tag for power. Hence the choice of using asynchronous logic for the Digital block becomes very obvious for our design. Asynchronous technique also favours modular design i.e. each of the module can be design separately and the whole modules can be assembled thereafter. Appropriate delay elements should be used to make the signals arrive at any point only when they are required.

Asynchronous Counter

The conventional method to transfer data in a digital system is to use a Shift Register. While for synchronous design various types of Shift Registers are available as Serial In Serial Out, Serial In Parallel Out, Parallel In Parallel Out and Parallel In Parallel Out. But for the asynchronous design the only type of Shift Registers reported till date is Serial In Serial Out and Serial In Parallel Out. Whereas in our design the data is available from the memory at the bit lines in parallel fashion and we need to sequence them to send it back. Hence we essentially need an asynchronous Parallel in Serial out Register which is not reported till date.

The only choice to derive the logic for fetching and transferring the data is to use a Counter. And asynchronous counters as readily available as basic building blocks in any literature. We also name it as Ripple Counter. Here it serves two fold advantages: one is to generate the input sequence for decoder to fetch the memory and generate selection lines for the MUX to sequence parallel data into serial one. Second, to generate all the sub-carrier frequency signals and the clock signal required for the coding of the data before transmitting it back.

We have an incoming frequency of 13.56 MHz at the clock. The data output rate as specified in ISO14443 regulations in 106 kbps i.e. 13.56 MHz/128. Hence we need a minimum of 7 (as 128=27) bit counters for it. But we derive the decoder input signals for fetching the memory from the same counter and also to sequence the parallel data available from the memory into serial form. Hence we have made a 14 bit asynchronous Up-Counter to implement the same. The whole 14 bit counter in two parts. Each T flip-flop acts as a divide-by-two counter. These T flip-flops have been made from standard D flip-flop with an asynchronous reset provided to initialize the states of all the flip-flops at the beginning of the operation. As depicted in the Fig. the last four outputs of the counter forms the counting sequence of 4 × 16 decoder. And the advantage of using T flip-flop lies in the fact that the inverting inputs to the decoder are also directly supplied by the same counter without any need of an inverter. But due to the finite propagation delay of the gates it is very obvious that the output of these counters will not arrive simultaneously to the input of decoder thereby giving rise to glitches which could false trigger the memory. Hence appropriate delay has been added in the path of each counting elements. Also as we go on adding the digital blocks in the circuit, the load capacitance becomes significant giving rise to unequal rise and fall times. This can further lead to glitches when logic of some block changes from high to low and for others low to high. So it is necessary to accordingly size the entire block of T flip-flop. After proper simulations we arrive with the sizes as mentioned in the Fig. For e.g. freq_div_14 means that the block is made 14 times larger in size than its smallest unit and so on.

From the last, leaving the output of four flip-flops, the next three are used to form the selection lines of 8 × 1 MUX used in our design. As the memory consists of 128 bits of data with 16 word lines and 8 bits lines, the output is available in the form of 8 parallel data bits every time the decoder input sequence changes. To order these into a serial manner we have used an MUX with these data bits as an input. These are selected one at time by the selection lines and are put the output. Since all the selection line inputs needs to reach the MUX at the same time instant, we have again added appropriate delays in their path as shown The data needs also to be coded with Manchester coding as specified in ISO 14443 Type A manuals. For coding we need a separate clock which is again derived from the counters which we have made for the decoder. The actual data rate comes after the coding which was earlier mentioned as 106 kbps or 13.56 MHz/128 and $128=2^7$. Hence it can be seen from the Fig. that the coding clock pulse is exactly derived from the output of 7th flip-flop. Again delay has been added in the form of inverter chain to synchronize it with the advent of data bits to the coding module. As mentioned earlier, all the uplink sub-carrier frequencies are also to be derived from the digital block. We can again obtain these from the counters. For ISO 14443 Type A specifications the sub-carrier frequency to be used for first level of ASK Modulation is 847 kHz or 13.56 MHz/16 and 16=24. Hence it is clearly seen from the Fig. that the signal for sub-carrier is taken from the 4th flip-flop of the counter with delay added in its path to compensate for the delay when the data arrives to the level one ASK Modulator with this sub-carrier.

2. Decoder

The decoder is the next main module of our digital block. Its function is to generate address for the memory to fetch the data and provide it to the bit lines. Since we have 16 × 8 ROM as memory, the output of decoder also contains of 16 lines giving rise to a 4 × 16 decoder. The figure shows the module of combined decoder and the ROM we have used in final schematic design. We can see that its input terminal come from the last four output of the counter as described earlier. Its output directly gives us the memory data on 8 bit lines V_Decod0-V_Decod15 to check its functionality.

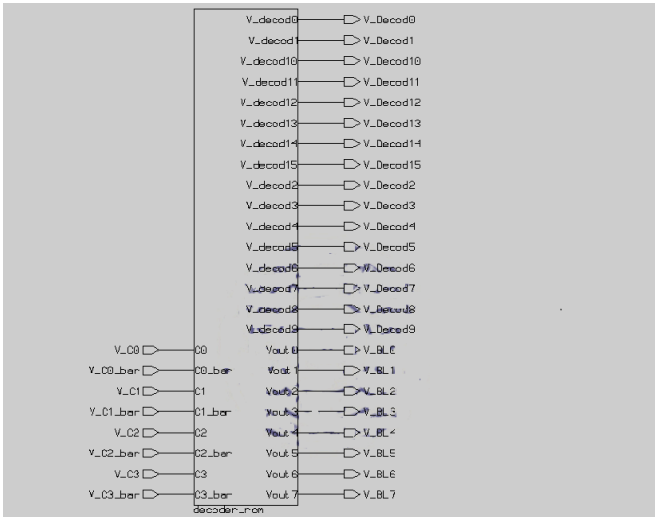

Figure 2 Decoder memory module schematic on IC STUDIO MENTOR GRAPHICS

Modular design

This technique requires a forming a simple module of four input NAND gates which could be repeatedly used to form a bigger modules and that bigger module to ultimately form the decoder this concept could be well understood if we look the counting sequence of the input at the decoder.

3. Memory

Memory is an important part of the tag because it contains the data stored in it. This data is the tag's identification which it has to transfer correctly to the reader to maintain its integrity. Also as large is the memory, power consumption increases as well size of the tag. In 13.56 MHz RFID System antenna is off-chip, so size is not major issue. But for passive tag on-chip power consumption does poses a serious issue. Hence memory design requires special attention.As our tag is read-only i.e. its just have to send its information to the reader, a simple ROM is sufficient. There are basically two types of MOS ROM are available in the literature, NOR ROM and NAND ROM. As it is obvious from their names, the pull-down devices neither work in NOR fashion in one type and as NAND in the other. In one the presence of pull down device forms a bit and in the other its

absence forms a bit. But the main factors to make a choice between them is the area occupied and time required to access them as the power consumption is almost same in both the cases. As taken from the Example 12.5 and 12.6 in the NAND ROM even after consuming less area takes delay in micro seconds to access it. Whereas NOR ROM works in nano seconds which is suitable for our work. So we finally use a 128 (16 × 8) bits MOS NOR ROM as shown in Fig. 3 below.The MOS ROM has been designed in conventional fashion i.e. keeping the size of all pull-down devices to minimum and using a very small W/L ratio for pull-up devices. This is because NOR ROM is made up of Ratioed Logic devices in which the pull-up network is always in on condition. So while accessing the memory the pull down network should be sufficiently be strong to overcome the strength of the pull-up network. Also we want minimum amount of power dissipation in the memory because once it gets powered up, current is continuously drawn from the pull-up network. Since we have used minimum sized transistors for the pull-down network, the only way to reduce the W/L of pull-up devices is to keep their W to minimum and increase the L as desired.In MOS NOR ROM the presence of transistor in pull-down network indicates a 0 bit where as absence means 1 bit. It is because as the word line WL goes high, corresponding device in pull-down network turns on and connect the bit line BL to ground. Whereas in the absence of pull-down device that bit line is already connected to pull-up device and hence goes high.

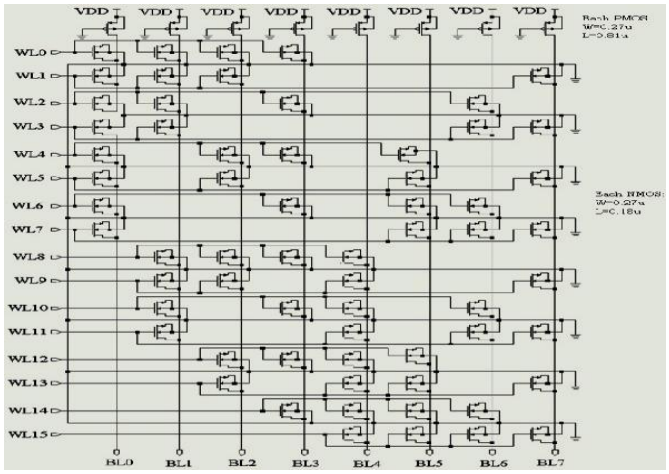

Figure 3 ROM 128(16X8) bits schematic on IC STUDIO MENTOR GRAPHICS

4. Multiplexer

The data available from memory is on bit lines with 8 sets of data simultaneously. But it needs to be sent in sequence one by one for transmitting back. Also with each word line, this 8 sets of data changes too. So we have to devise some mechanism to transfer this data before the next set comes in. The usual procedure for its implementation is to use a Shift Register. But then it calls for design to be synchronous. Whereas from our asynchronous counters which we have already, we can easily derive functions to selectively transfer the data using a multiplexer.

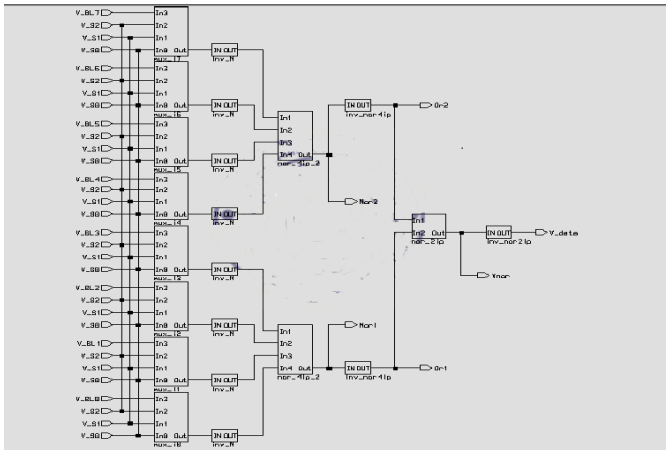

Figure 4 Multiplexer schematic on IC STUDIO MENTOR GRAPHIC

Simulation and Result

Asynchronous Counter

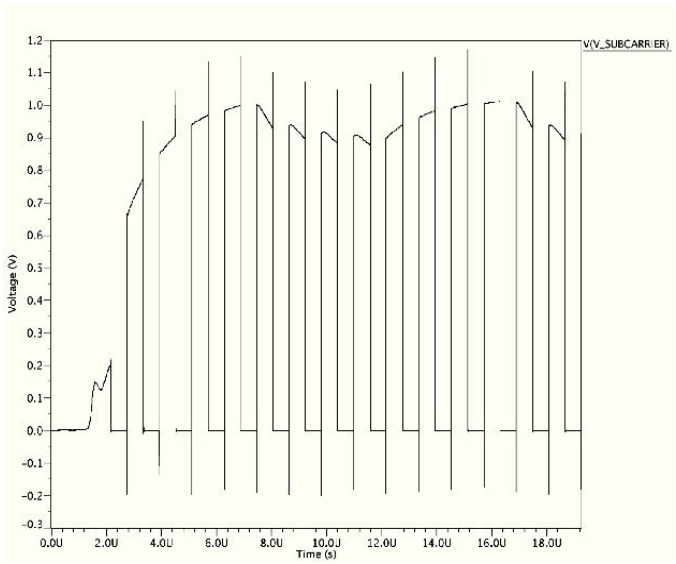

Figure 4.26 Asynchronous Counter output for subcarrier zoomed on EZ WAVE MENTO GRAPHICS

The subcarrier is obtained as shown above. The difference between one period equals 1.18421 µs giving frequency as 844.45 kHz which is almost equal to the specified subcarrier of 847 kHz in ISO 14443 Type A regulations.

Decoder

The decoder output is as shown for all of its 16 output lines. The duration for which one output should be high is the total simulation time divided by the no. of outputs i.e. 1228.8 µs / 16 = 76.8 µs. Hence this becomes the time for which the outputs are available at the bit lines of the memory and the MUX needed to complete it one cycle of operation. Alternatively, this could also be determined by the time period of the slowest selection lines of the MUX which is already calculated earlier as 76.8 µs for the signal V_S2. The above pulse width could also be verified from the graphs plotted.

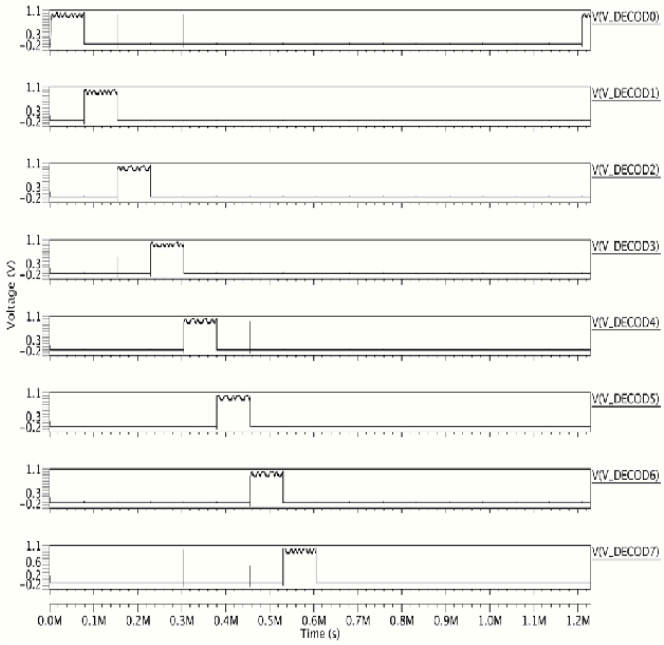

Figure 4.27 Decoder output (Part 1) on EZ WAVE MENTOR GRAPHICS

Multiplexer

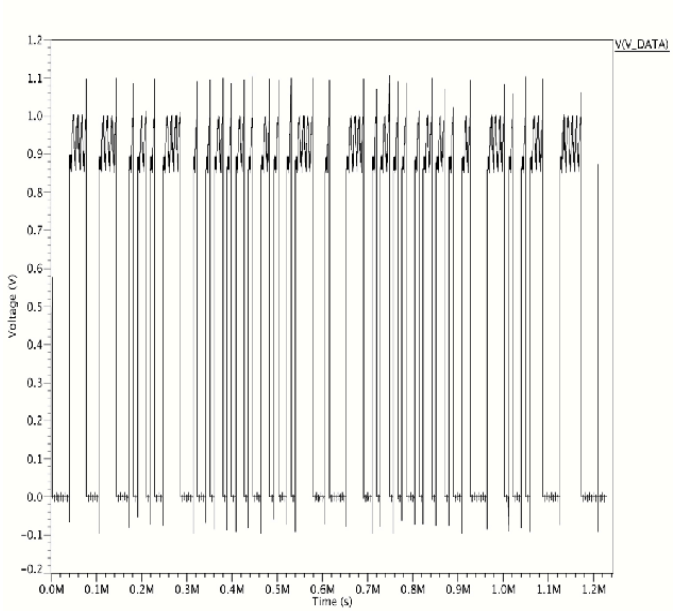

Figure 4.29 Multiplexer output on EZ WAVE MENTOR GRAPHICS

The MUX sequences the data available from the memory which is shown as above. But the data needs to be verified accurately because for two reasons: one as it is the tag's identity, so if it is not acquired properly then our design will be discarded and second that this is the last stage where we can check the authenticity of the stored data as after this stage it will be encoded and modulated. Hence in the following graphs we check all the 8 bit lines output when a word line is high.

5. CONCLUSIONS

A low cost low power Digital block of RFID tag has been designed and simulated for the intended application. The application depends upon the read range of the RFID system which is 7-15 cm in our case. Hence, our tag could be used in banking sector or library management system where the operation could be completed within this range. The result shown matches the simulation result of a typical ISO 14443 compliant Type A RFID tag described in [3]. The data rate achieved is same as specified in ISO 14443 i.e. 106 kbps. A 10% ASK modulation has been achieved which was as required for our design. The digital rail to rail voltage has been slightly dipped from 1V due to power scarcity. But till this voltage is above the noise margins of the digital circuit, their functionality is achieved. Also the design is suitable to operate at the rms voltage i.e. 2.581V available at the Hmin of the reader's field strength as discussed earlier. Each and every bit of the ROM has been extracted and tested at the output. We have successfully performed the memory fetch operation with high fidelity. The idea to implement digital block in asynchronous logic has proved satisfactory from the simulation results of the digital schematic. Hence we can say that we have successfully achieved the desired results which we had expected from our design with reduced complexity and low power.

6. ACKNOWLEDGMENT

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