RESEARCH INVENTY: International Journal of Engineering and Science
ISSN: 2278-4721, Vol. 1, Issue 6 (October 2012), PP 07-13
www.researchinventy.com

STUDY & ANALYSIS OF ENCODER FOR VLSI INTERCONNECTS

Anubha Chauhan
Department of Computer Science and Engineering,
G. B. Pant Engineering College, Pauri-Garhwal, INDIA

ABSTRACT:
For System on-chip (SOC) designs in current Deep Submicron (DSM) era, the performance factors such as propagation delay, power dissipation and crosstalk in RC modeled interconnects are the major design concerns. The crosstalk effect is a consequence of coupling and switching activities that is encountered when there is a transition in previous state of wire as well as when there are transitions in adjacent wires. Therefore, minimization or elimination of switching and coupling activities is crucial in enhancing the performance of SOC designs. This paper proposes encoding scheme to achieve overall reduction in transitions. The reduction in transition improves the performance in terms of reduced power dissipation, coupling activity and delay in on-chip buses.

KEYWORDS: *COUPLING, VLSI, SOC, BUS ENCODING, INTERCONNECTS.*

I INTRODUCTION

The feature size of integrated circuits has been consistently reduced in the pursuit of improved speed, power, silicon area and cost characteristics. Semiconductor technologies with feature sizes of several tens of nanometers are currently in development. As per International Technology Roadmap for Semiconductors (ITRS), the future nanometer scale circuits will contain more than a billion transistors and operate at clock speeds well over 10GHz. Distribution of robust and reliable power and ground lines; clock; data and address; and other control signals through interconnects in such a high-speed, high-complexity environment, is a challenging task.

The function of wiring systems or interconnects is to distribute clock and other signals and to provide power/ground to and among the various circuits/systems functions on the chip. The performance parameters i.e. time delay and power dissipation of a high-speed chip is highly dependent on interconnects, which connect different macro cells within a VLSI chip.

In current DSM (Deep Submicron) technology, coupling capacitance plays an important role for deciding the behavior of on-chip interconnects. Due to the coupling capacitance, crosstalk, delay and power consumption problems will arise.

The above problems are very much dependent on the frequency of signal used, length of interconnects etc. Interconnects can be modeled as the transmission line. Transmission line may be modeled as *RC* or *RLC* network.

The effect of inductance plays an important role as the length and used frequency signal increases. [1-4, 8-16] This paper considers *RC* network for the implementation and study of the behavior of interconnects due to coupling capacitance. The components that affect the behavior of the on-chip bus are internal parasitic capacitances of the transistors, interconnect capacitances and input capacitances of the fan-out gates.

The most common methods to reduce crosstalk, propagation delay and power are:

- Insertion of repeaters
- Insertion of shielding between adjacent wires
- Minimizing spacing between signal and ground lines.
- Isolating clocks and other critical signals from other lines (larger line spacing) or isolation with ground traces.
- In backplane or wire-wrap applications, use twisted pair for sensitive applications such as clocks and asynchronous set or clear functions. While using ribbon or flat cable, make every other line a ground line.
- Introduction of intentional delay among coupled signal transmission.
- Bus Encoding methods

- The use of tight geometry in most systems can reduce crosstalk significantly although it cannot eliminate it entirely. Some preventive design measures can be used to minimize crosstalk.
- Using maximum allowable spacing between signal lines.
- Terminating signal lines into their characteristic impedance.

The encoding method is widely used technique to reduce dynamic switching power and the effects of crosstalk (signal noise, delay) during data transmission on buses. Low power encoding techniques aim to transform the data being transmitted on buses in such a manner so that the self and coupling switching activity on buses are reduced. Crosstalk aware encoding techniques can also modify the switching patterns of a group of wires to reduce crosstalk coupling effect. These techniques are quite effective in reducing power consumption, improving transmission reliability, and increasing system performance. For any encoding scheme, the encoder and decoder functions are the inverse of each other. Bus encoding schemes can be classified according to several criteria, such as the amount of extra information needed for coding (redundant or irredundant coding), and the method of encoding implementation (hardware, software, or a combination of the two), Type of code used (algebraic, permutation, or probability based), the degree of encoding adaptability (static or dynamically adaptable encoding), the targeted capacitance for switching reduction (self, coupling or both).

Encoding techniques are often aimed at power reduction, signal transmission delay reduction and reliability improvement, or a combination of these due to the reduction in the transition. Certain optimizations such as crosstalk reduction can have multiple benefits associated with them such as power reduction, signal delay reduction and noise reduction.

This paper presents an encoding method for the reduction of coupling transitions. The crosstalk is classified as the types depending upon the transitions of the signal in the wire. This paper proposes encoding schemes which reduces data lines hence there is reduction in power consumption. The encoding scheme presented in the paper reduced the redundancy. It also considers the worst case crosstalk effects due to transitions in the group of lines.

II Estimation Of Power And Crosstalk In Rc Bus Model

The total power consumption in the VLSI chip comprises of dynamic power, short circuit power, static power and leakage power. It can be simply described as summation of all these components.

$$P_{Dissipation} = P_{Static} + P_{Dynamic} + P_{Leakage} + P_{Shortckt} \quad (1)$$

The capacitance of interconnect can be classified as coupling capacitance and self capacitance. The coupling capacitance is the capacitance between the adjacent wires while the self-capacitance refers to the capacitance between the substrate and the wire itself. The dynamic power in VLSI chip decides the behavior of chip and is highly dependent on the load capacitance and coupling capacitance i.e. bus line signal transitions.

$$P_{D,Coded} = (\alpha_{cl} \times C_L + \alpha_{cc} \times C_C) \times {V_{DD}}^2 \times f$$
$$= (\alpha_{cl} + \alpha_{cc} \times \lambda) \times C_L \times {V_{DD}}^2 \times f) \quad (2)$$

Dynamic power dissipation on a coded bus thus can be defined as following equation (2) where *CL* is the load capacitance, *Cc* is the coupling capacitance, *VDD* is the supplying voltage, is the clock frequency, λ is the capacitance ratio defined as: $\lambda = Cc / CL$. Λ is dependent on the technology which is being used hence its value depends on the physical parameters. αcl is the value of average switching activity for the load capacitance. For un-encoded buses αcl is 1. αcc is the value of average coupling activity for the coupling capacitance. For un-encoded buses αcc is 1. Hence for un-encoded data the power dissipation can be defined by following equation (3)

$$P_{D,un-coded} = (1 + \lambda) \times C_L \times {V_{DD}}^2 \times f \quad (3)$$

Effective crosstalk capacitance is determined by (4)

$$C_{eff} = C_c \times \frac{\Delta V_2 - \Delta V_1}{V_{DD}} + C_C \times \frac{\Delta V_2 - \Delta V_3}{V_{DD}} \quad (4)$$

Where $\Delta V2$ is voltage variation of the centre wire is $\Delta V1$ and $\Delta V3$ are voltage variations in the adjacent wires are power supply voltage which equals rail-to-rail signal voltage in CMOS circuits is effective coupling capacitance variation [1, 2].

The coupling between the groups of the three wires is classified into five types depending upon the nature of transitions of signals in the wire that are Type-0, Type- 1, Type-2, Type-3 and Type-4. The Type-0 coupling occurs when all of the 3-bit wires are in the same state transition. A transition from 000 to 111 (i.e. ↑↑↑) causes a Type-0 coupling. For Type-0, coupling capacitance is zero. Type-1 coupling occurs when there is a transition in one or the two wires (including the centre wire) and the third wire remains quite. There are eight possibilities by which Type-1 condition occurs. The coupling capacitance in this case is.

A Type-2 coupling occurs when the centre wire is in the opposite state transition with one of its adjacent wires while the other wires undergo the same state transition as the centre wire i.e.100 to 011. Ten different conditions are possible for Type-2 coupling. The coupling capacitance is 2 in this case. A Type-3 coupling occurs when the central wire undergoes the opposite state transition with one of the two wires while the other wires are quiet i.e. 010 to 001. Coupling capacitance in the case of Type-3 coupling is 3 and there are four possibilities that cause Type-3 coupling. For a Type-4 coupling, all three wire transitions are in the opposite states with respect to each other. Two conditions cause Type-4 coupling with a coupling capacitance effect of 4. All the five Types of couplings are shown in Table-1 [2].It can be concluded from the above description that power and crosstalk highly depend upon the transitions of the signal in the wires. If the number of transitions occurring in the signals by encoding methods is reduced, the dynamic power dissipation as well as crosstalk will also be reduced. Different encoding methods are proposed by different researchers. An efficient encoding proposed by Stan and Burleson [3] includes the concept of counting the number of transitions, with respect to the previous states of group of lines. Data is transmitted in original form or in inverted form depending upon the number of state transition of the lines as compared to previous states.

Table 1. Crosstalk Types for a 3-Bit Bus Considering *RC* Model of Interconnect [2]

Type-0	Type-1	Type-2	Type-3	Type-4
– – –	– –↑	–↑–	–↑↓	↑↓↑
↓↓↓	–↑↑	↑–↑	–↓↑	↓↑↓
↑↑↑	↑––	↑–↓	↑↓–	
	↑↑–	↑↑↓	↓↑–	
	– –↓	↑↓↓		
	–↓↓	–↓–		
	↓––	↓–↓		
	↓↓–	↓–↑		
		↓↓↑		
		↓↑↑		

↑: switch from "0" to "1", ↓: switch from "1" to "0", - : no transition

III Encoding Method

The proposed encoding method transforms the bus signals for the reduction or elimination of the worst case crosstalk by reducing the 7-bit lines into 4-bit lines. The encoder deals with the coupling transitions among the group of seven bits. It identifies the higher number of 0's and 1's. Output line is set according to higher number of 0's or 1's. The proposed encoder can be depicted as in Fig.1. The components of the encoder circuit include a counter module, controller, a 7-bit comparator module, multiplexers and buffers. Firstly, the number of 0's and 1's are counted using a counter module. If the number of 0's is more than the number of 1's, the comparator module sets output line in low state (0). If the number of 1's is more than the number of 0's, this module sets output line in high state (1).

There are two best cases possible; either all lines are in one state or all lines are in zero state. As said earlier, it is needed to convert all the seven input lines to a single line, either 0 or 1. In order to do this, the position of bits are flipped to either 0 or 1 depending upon the value of 0's or 1's, whichever is higher as discussed above. There are maximum three flips possible.

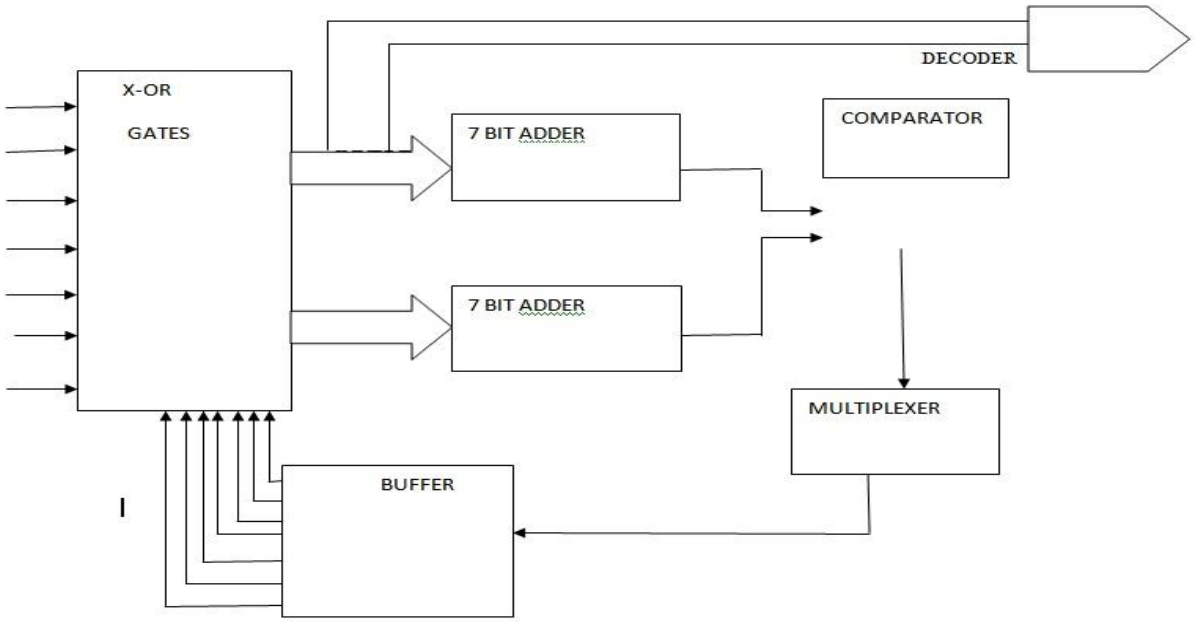


Fig. 1. Block Diagram of Encoding Method

The single output line of controller is compared with initial 7-bit input line and finds the flipped bit positions. The number of flipped bits could be 0 (best case; when all the inputs are either 0 or 1), or 1 or 2 or 3 (worst case), after identification of the flipped bits positions, and stored in the multiplexer. The multiplexer is chosen to be three in order to work for the best as well as the worst cases. The best case is one when all the input lines are 0 or 1. Thus there is significant reduction in crosstalk as all have same null value. Seven bits of input have been given to the encoder. So, three bits have taken to indicate the flips in the seven lines. All the equivalent positions for these 8 combinations are shown in Table 2.

Table 2. Register Values Indicating the Positions of Flipping

Register Value	Flipped I/P Line Position
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Each value sends in three different clock cycles. At each clock cycle, contents are sent to the decoder. Other contents are sent in the next clock cycle and so on. Since the maximum flips that can be possible are three so maximum three clock cycles are required for decoding the 7-bit line at decoder side.

3.1. COUNTER MODULE

The counter module is for the determination of the number of 0's and 1's in the input sequence of seven bits line. The input to the counter module is 7-bit input. Each of these lines is selected and then compared with '0' and '1'. Two variables are initialized for storing the values of the number of 0's and 1's in the input sequence. The first variable stores the value of the number of 0's and the other one store the number of the 1's in the input sequence. These two lines are then fed into the Controller modules along with two variables and are passed to the Controller; it then decides whether the number of value of 1st or the 2nd variable is higher. The one with higher value is forwarded to the comparator module of the encoder.

3.2. CONTROLLER

As seen in Fig.1 the two output lines of the counter represent the number of 1's and the number of 0's. These two inputs are fed in to the controller. The Controller decides for the number of occurrences of 0's and 1's as provided by counter module.

This module decides the output as '0' or '1' based on the values input to this. If number of 0's is higher as compared to the number of 1's the output of the controller will be '0'. If number of 1's is higher as compared to the number of 0's the output of the controller will be '1'.

3.3. COMPARATOR

The single output line is fed to the comparator along with the invert 7-bit inputs. This single output line is compared with each of the initial 7-bits. This is to compare whether the value of the bit is the same or different from the single line. This signal is XORed with each of the 7 lines to identify the flipping.

These flipped positions are stored for the decoding purpose. The final output of this as discussed before are meant for transfer of the three flipped positions if present or whatever the number of flipped bit positions is from 0 to a maximum of 3 positions.

3.4. MULTIPLEXER

The multiplexer is a special combinational circuit that is one of the most widely used standard circuits in digital design. The multiplexer (or data selector) is a logic circuit that gates one out of several inputs to a single output. The input selected is controlled by a set of select inputs.

These lines along with the single input equivalent line from the controller are transmitted to the decoder. The encoder provides the output in four lines for the decoding purpose i.e. one line from the controller and the other three lines from the register, although three clock cycles are needed for complete decoding of the input sequence.

3.5. BUFFER

The buffer circuits at the input are required to limit loading of the sources that drive the inputs. It produces inverted as well as non inverted inputs at the output. Output buffers are required to increase the driving capability of the PLA. Usually, the outputs are TTL compatible. The outputs may be totem-pole, open collector, or three-state.

IV Decoder

The decoder of the proposed encoding method is shown in Fig.2. The decoder of the proposed encoding method consists of the 2*1 multiplexer, buffer, splitter, x-or gate and line identifier. Four lines from the encoder are fed to the decoder. In the first clock cycle the contents of the first value from encoder are stored in the multiplexer of the decoder and so on. The maximum flips that can be possible are three, so maximum three clock cycles are required for complete decoding of the 7-bit data.

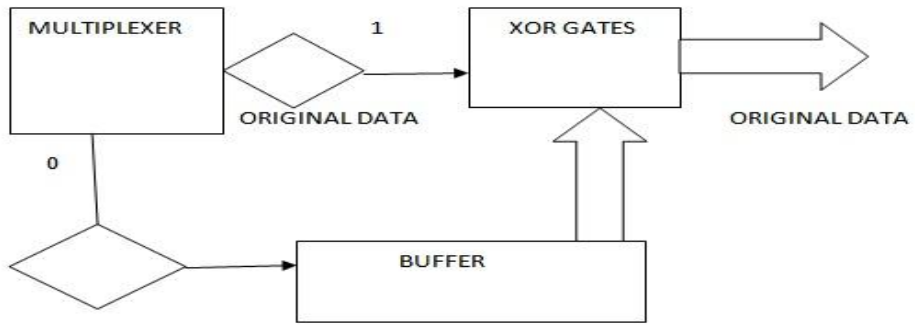


Fig. 2. Decoder of Encoding Method

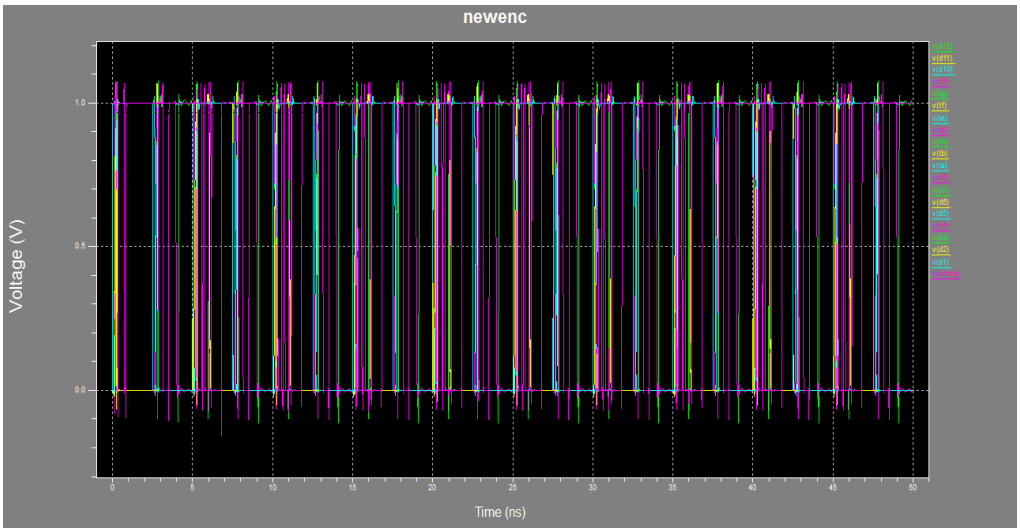
Although, 2*1 multiplexer can be used in the encoder and decoder side instead of three 3-bit registers, multiplexer is used for the compensation of delay generated by the clock cycles for the transmission of flipped bit positions to decoder side. The output line taken from the comparator of encoder side is fed to the splitter module of the decoder. The splitter module splits the 1-bit input line to seven bits of output lines. All the seven output lines have similar value as that of the input i.e. if the input to the splitter is '1' then output of the splitter is of seven lines having value of each line as '1'. Similarly when input of the buffer is '0' all the seven lines will

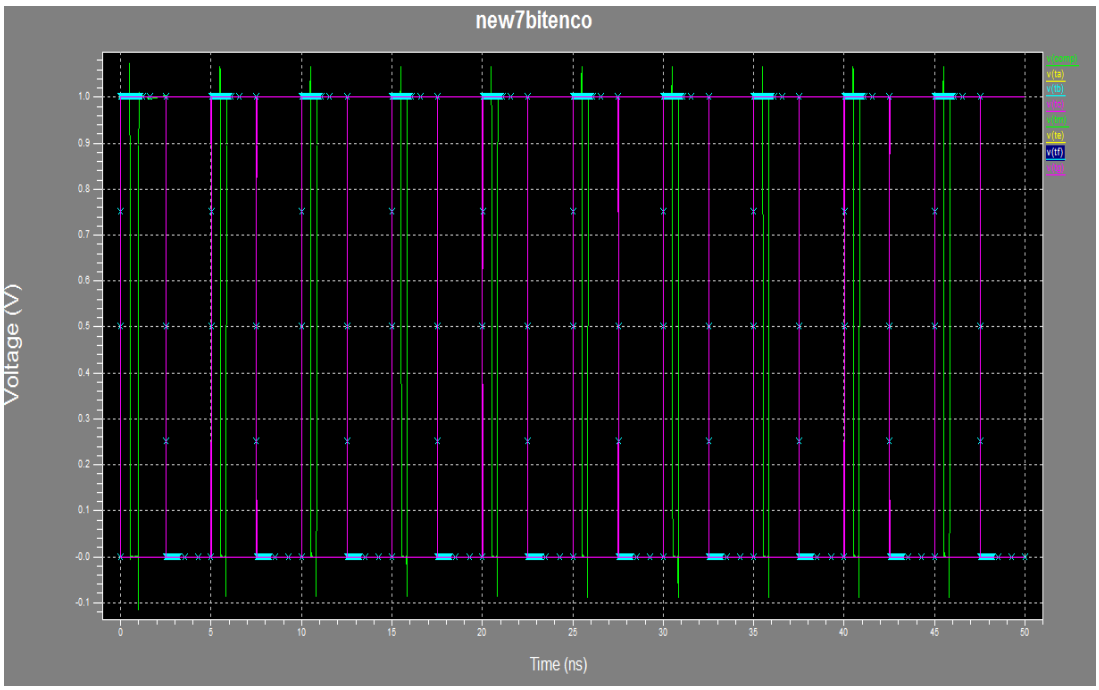
have output value ’0’. The sequence is managed by the clock cycle. Line identifier gets the content of multiplexer and identifies the line to be flipped as per Table 2. These identification indications are then fed to the x-or gate. This compares the indentified line. In next turn this process is repeated. And after three iterations the final decoded data of seven bits is taken as the output of the decoder.

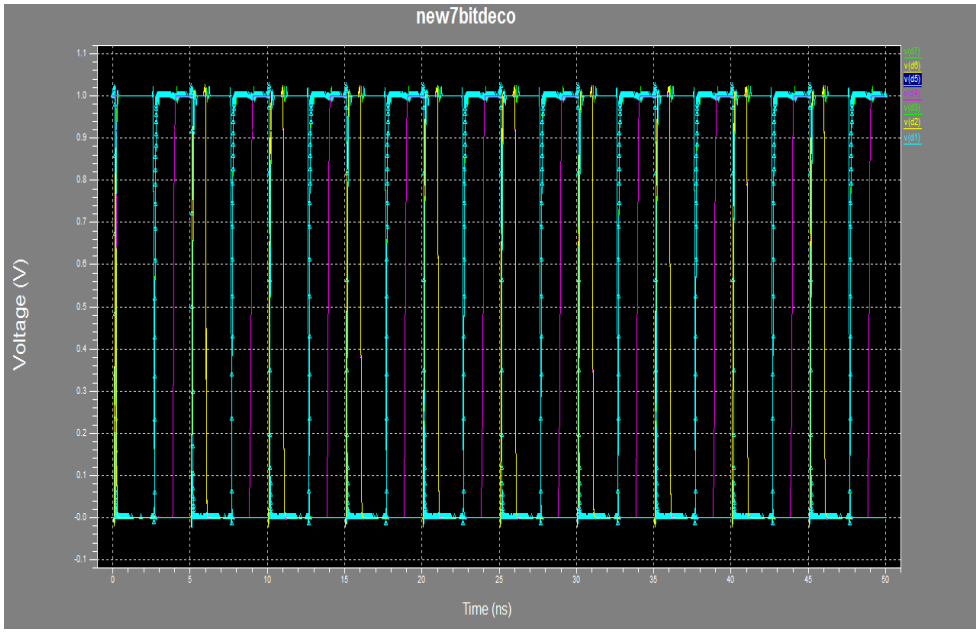
V Simulation And Results

Encoder and decoder are implemented in T-Spice. In the encoder described in the previous sections have a 7-bit input sequence and the task was to reduce the crosstalk and power dissipation using bus encoding schemes. The designed encoder reduces the 7-bit input sequence to a 4-bit output sequence. This encoding scheme not only reduced the redundancy but reduced the power consumption too, after the implementation of encoding mechanism. The encoder is tested on the random 7-bit sequences and it was found that the worst case crosstalks get reduced. There was also a decrease in power dissipation as compared to the initial sequence. Further, as two out of the three parameters, i.e. power dissipation and crosstalk are decreased, the delay is introduced.

This delay can therefore be allowed as the overall implementation is better than the initial input sequence transmission method. Hence, it is evident that this method is acceptable. This encoder considers only the coupling transitions in the input 7-bit sequence.







VI Conclusion

The proposed method of bus encoder significantly eliminates or reduces the worst case crosstalk. Reduction of crosstalk is because of the reduction in the number of lines from 7 bits to 4 bits as an output of the Encoder. This reduces the crosstalk effectively by 35 to 40 percent. The transitions in the state of buses decide the behavior of the switching and coupling activities. It is shown that reduction in the coupling and switching activity reduces the dynamic power dissipation and crosstalk. Thereby the power dissipation is also reduced as compared to the initial input sequence. Hence the performance of the VLSI chip is improved. For all possible 128 combinations of the input sequence the output is seen manually and via the implemented mechanism. It is finally found that the method is implemented successfully and serves its purpose to a great extent.

References

[1] Duan, C., Calle, V.H.C., Khatri, S.P.: Efficient On-Chip Crosstalk Avoidance CODEC Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 17(4), 551–560 (2009) ISSN: 1063-8210

[2] Khan, Z., Arslan, T., Erdogan, A.T.: A Low Power System on Chip Bus Encoding Scheme with Crosstalk Noise Reduction Capability. IEEE Proc. Computer & Digital Techniques (2005)

[3] Stan, M.R., Burleson, W.P.: Bus-invert coding for low power I/O. IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 49–58 (1995)

[4] Shin, Y., Chae, S., Choi, K.: Partial Bus-Invert Coding for Power Optimization of System Level Bus. In: Proceedings of the 1998 International Symposium on Low Power Electronics and Design, pp. 127–129 (1998)

[5] VHDL Reference Guide, Xilinx, Inc. (1999), (http://toolbox.xilinx.com/docsan/)

[6] Perry, D.L.: VHDL, Programming by example, 4th edn. McGraw-Hill, New York

[7] Mano, M., Kime, C.: Logic and Computer Design Fundamentals, 2nd edn. Prentice Hall, Upper Saddle River (2001)

[8] Aghaghiri, Y., Fallah, F., Pedram, M.: Transition reduction in memory buses using sector based encoding techniques. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 23(8), 1174–1184 (2004)

[9] Satyanarayana, N., Vinaya Babu, A., Mutyam, M.: Delay-efficient bus encoding techniques. Microprocessors & Microsystems 33(5-6), 365–373 (2009)

[10] Lin, T., Shang, T., Jou, J.: On-Chip Bus Encoding for Power Minimization under Delay Constraint. In: IEEE International Symposium on VLSI Design, Automation, and Test, VLSI-DAT (2007)

[11] Kaushik, B.K., Sarkar, S.: Crosstalk Analysis for a CMOS-Gate-Driven Coupled Interconnects. IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems 27(6), 1150–1154 (2008)

[12] Kaushik, B.K., Sarkar, S., Agarwal, R.P.: Waveform Analysis and Delay Prediction for a CMOS Gate Driving RLC Interconnect Load. Integration, the VLSI Journal 40(4), 394–405 (2007)

[13] Kaushik, B.K., Sarkar, S., Agarwal, R.P., Joshi, R.C.: Crosstalk Analysis of Simultaneously Switching Interconnects. International Journal of Electronics 96(10), 1095–1114 (2009)

[14] Kaushik, B.K., Sarkar, S., Agarwal, R.P., Joshi, R.C.: Effect of Line Resistance and Driver Width on Crosstalk in Coupled VLSI Interconnects. Microelectronics International 24(3), 42–45 (2007)

[15] Verma, S.K., Kaushik, B.K.: Encoding Schemes for the Reduction of Power Dissipation, Crosstalk and Delay: A Review. International Journal of Recent Trends in Engineering 3(4), 74–79, ISSN 1797-9617

[16] Verma, S.K., Kaushik, B.K.: Reduction of transitions in RC coupled systems in VLSI interconnects. In: International Conference on Emerging Trends in Engineering & Technology ICETET, pp. 735–740. IEEE Computer Society, Los Alamitos (2010)